

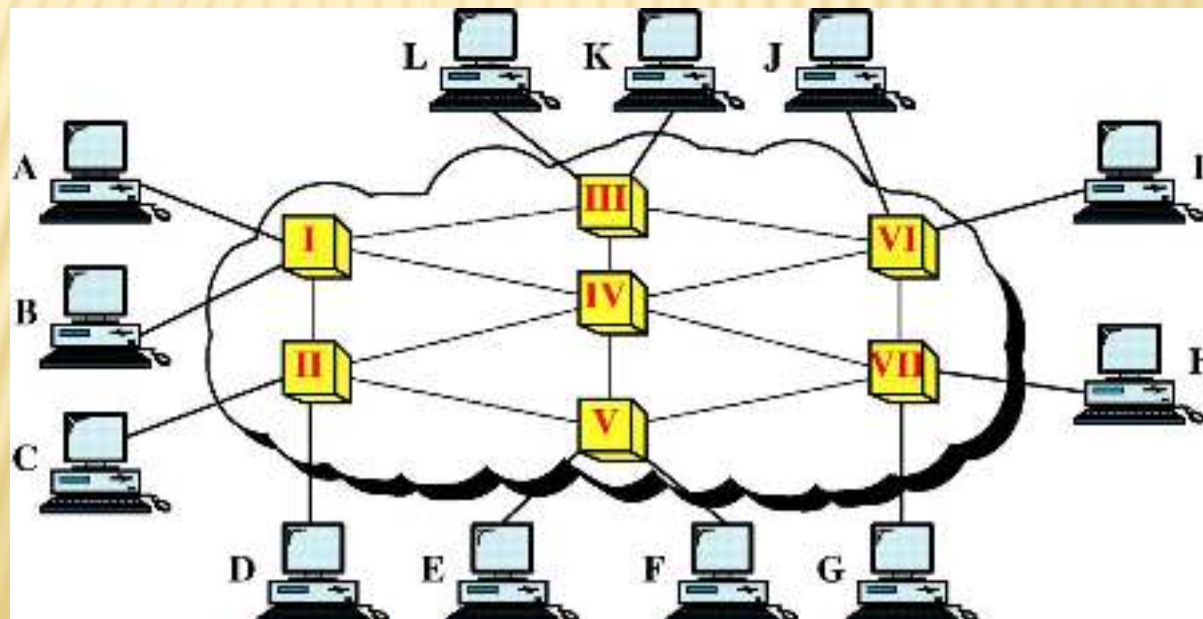
BROADBAND AND HIGH SPEED NETWORKS

2 Network switch Switching

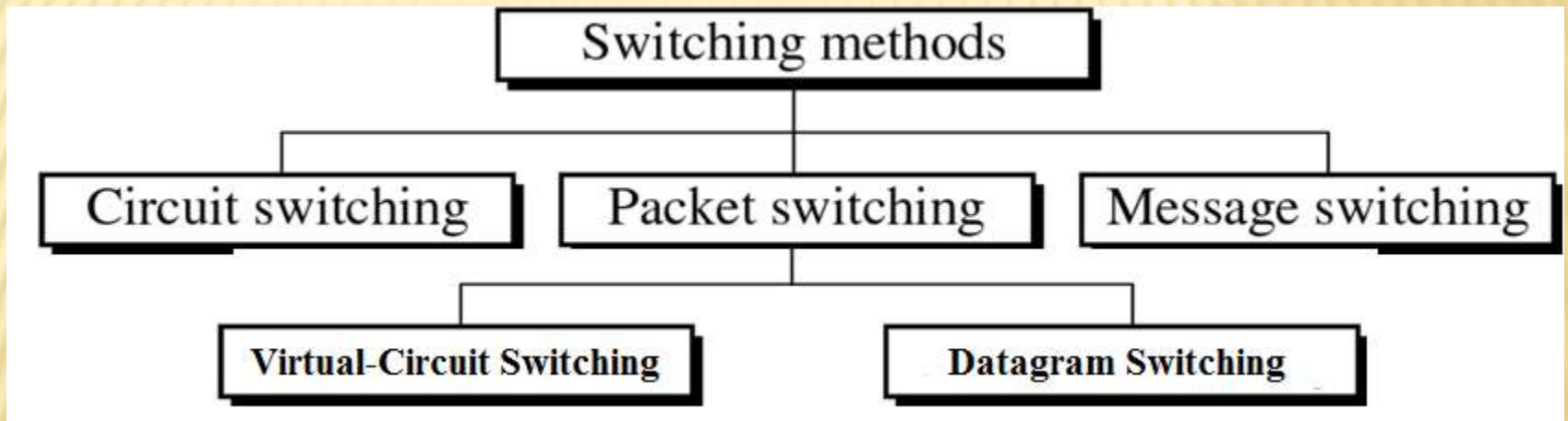
SWITCHING

A switch is a mechanism that allows us to interconnect links to form a larger network. A switch is a multi-input, multi-output device, which transfers packets from an input to one or more outputs.

A switched network consists of a series of interlinked nodes, called switches. Switches are devices capable of creating temporary connections between two or more devices linked to the switch. In a switched network, some of these nodes are connected to the end systems (computers or telephones, for example). Others are used only for routing.



SWITCHING NETWORK CATEGORIES



CIRCUIT-SWITCHED NETWORK

A **circuit-switched network** consists of a set of switches connected by physical links.

- A connection between two stations is a dedicated path made of one or more links (channels).
- Each link is normally divided by using FDM or TDM into n channels .

Time-division multiplexing (TDM) is a method of transmitting and receiving independent signals over a common signal path by means of synchronized switches at each end of the transmission line so that each signal appears on the line only a fraction of time in an alternating pattern.

Frequency-division multiplexing (FDM) is a technique by which the total bandwidth available in a communication medium is divided into a series of non-overlapping frequency sub-bands, each of which is used to carry a separate signal. These sub-bands can be used independently with completely different information streams, or used dependently in the case of information sent in a parallel stream.

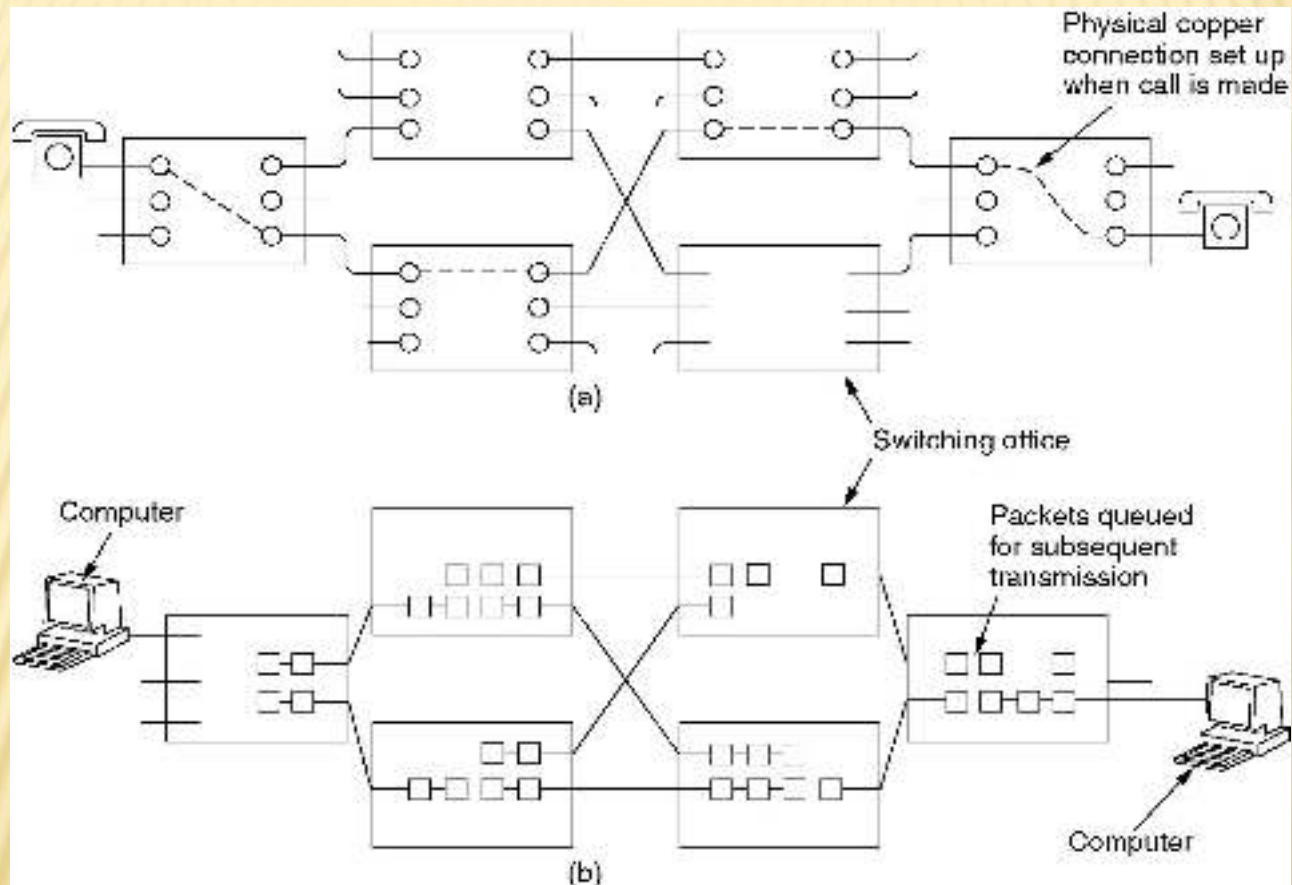
The actual communication in a circuit-switched network requires three phases:

- Connection setup,
 - Data transfer, and
 - Remove connection.
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- Circuit switching takes place at the physical layer.
 - Before starting communication, the stations must make a reservation for the resources to be used during the communication.

These resources, such as channels (bandwidth in FDM and time slots in TDM), switch buffers, switch processing time, and switch input/output ports, must remain dedicated during the entire duration of data transfer until the teardown phase.
 - Data transferred between the two stations are not packetized (physical layer transfer of the signal). The data are a continuous flow sent by the source station and received by the destination station, although there may be periods of silence.
 - No addressing involved during data transfer. The switches route the data based on their occupied band (FDM) or time slot (TDM). There is end-to-end addressing used during the setup phase.

PACKET-SWITCHED NETWORK

- ❖ **Packet-switched Network** is a digital networking communications method that groups all transmitted data into suitably sized blocks, called packets. Variable-bit-rate data streams (sequences of packets) delivered over a shared network. When traversing network adapters, switches, routers and other network nodes, packets are buffered and queued, resulting in variable delay and throughput depending on the traffic load in the network.
- ❖ Packet switching contrasts with circuit switching, a method which sets up a limited number of dedicated connections of constant bit rate and constant delay between nodes for exclusive use during the communication session. In case of traffic fees, for example in cellular communication services, circuit switching is characterized by a fee per time unit of connection time, even when no data is transferred, while packet switching is characterized by a fee per unit of information.



(a) Circuit switching

(b) Packet switching

PACKET-SWITCHING NETWORKS

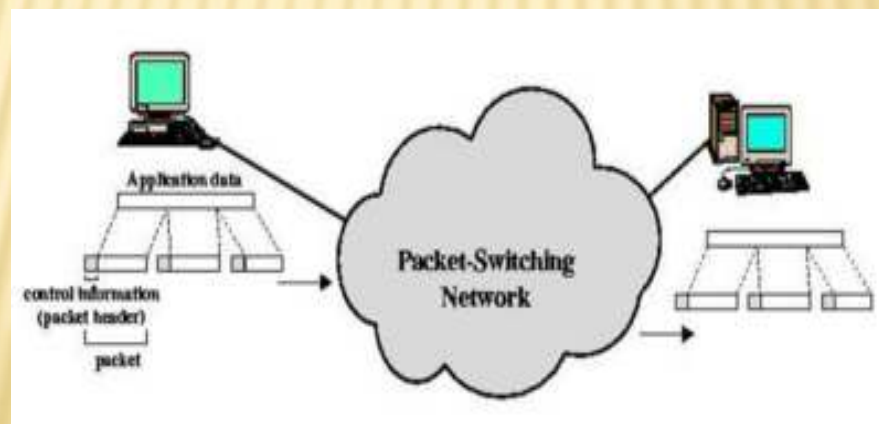
- ❑ One of the few effective technologies for long distance data communications
- ❑ Frame relay and ATM are variants of packet-switching

Advantages:

- flexibility, resource sharing, robust, responsive

Disadvantages:

- Time delays in distributed network.
- Need for routing and congestion control



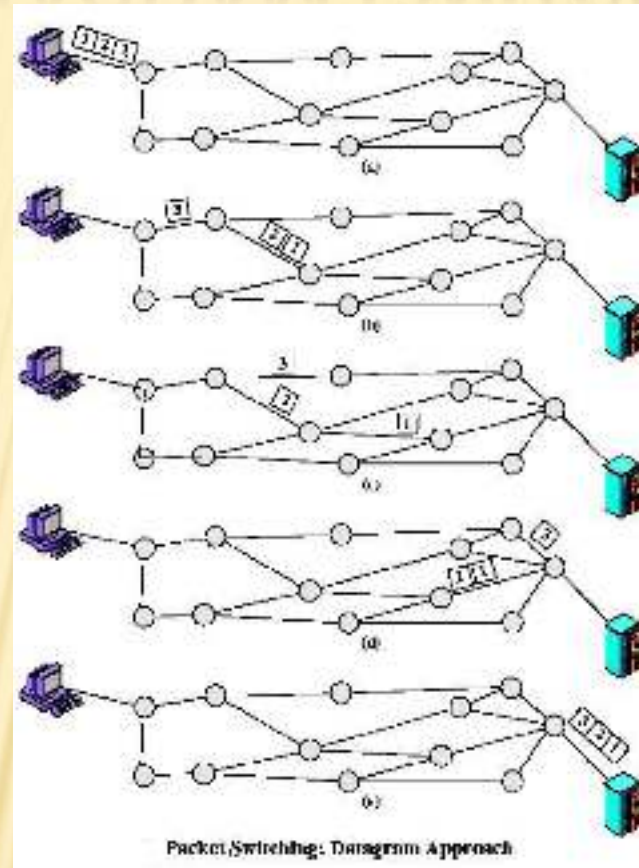
The Use of Packets

TWO MAJOR PACKET SWITCHING MODES :

(1) connectionless packet switching, also known as datagram switching:

Each packet includes complete addressing or routing information. The packets are routed individually, sometimes resulting in different paths and out-of-order delivery.

DATAGRAM SWITCHING



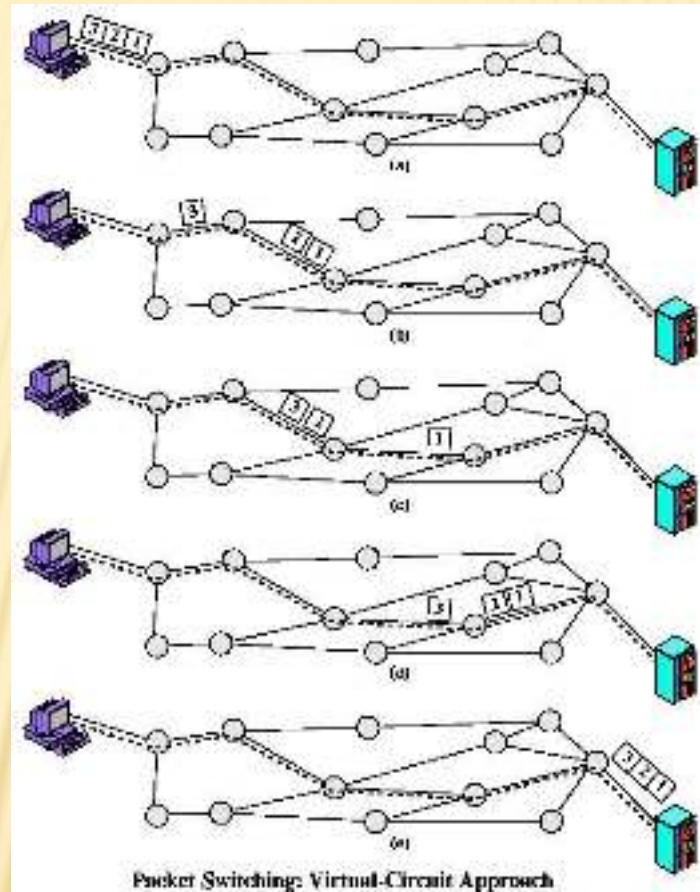
Datagram

- ❖ Each packet sent independently of the others
- ❖ No call setup
- ❖ More reliable (can route around failed nodes or congestion)

(2) connection-oriented packet switching, also known as virtual circuit switching

A connection is defined and pre allocated in each involved node during a connection phase before any packet is transferred. The packets include a connection identifier rather than address information, and are delivered in order.

VIRTUAL CIRCUIT SWITCHING



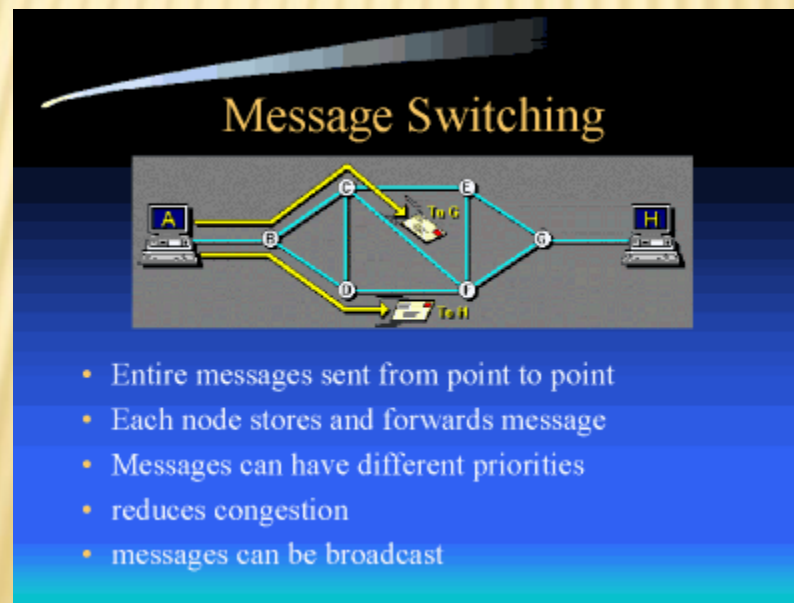
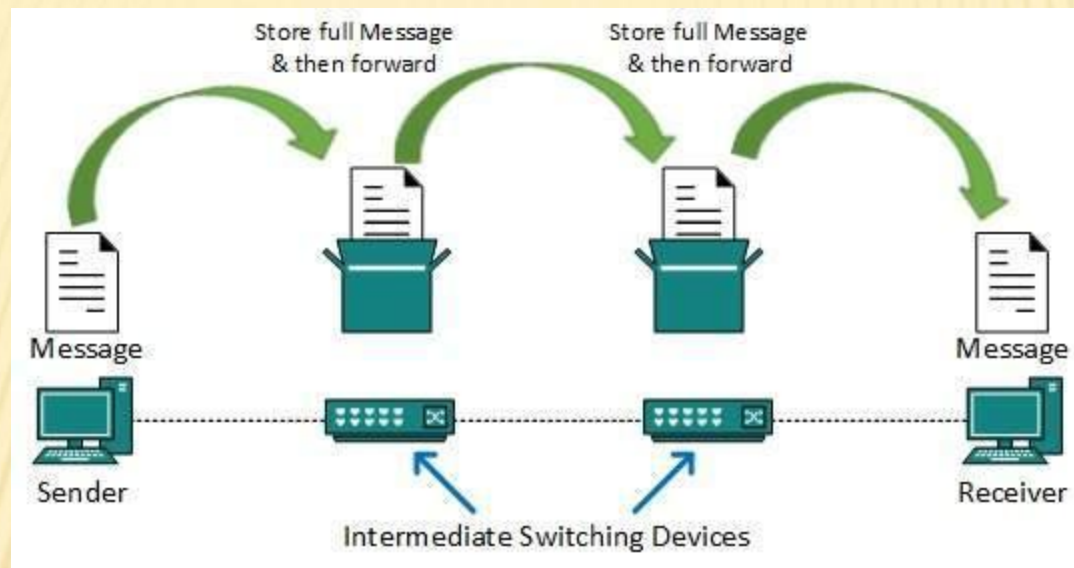
Virtual circuit

- ❖ Fixed route established before any packets sent
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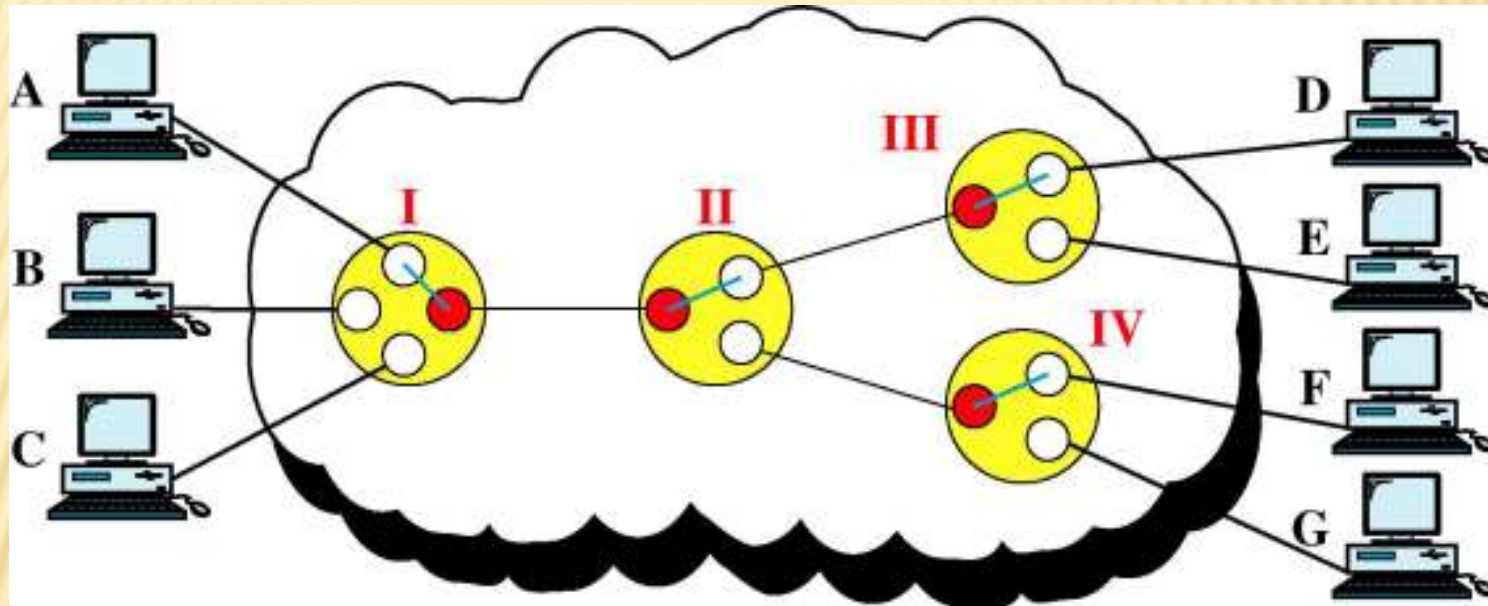
MESSAGE SWITCHING

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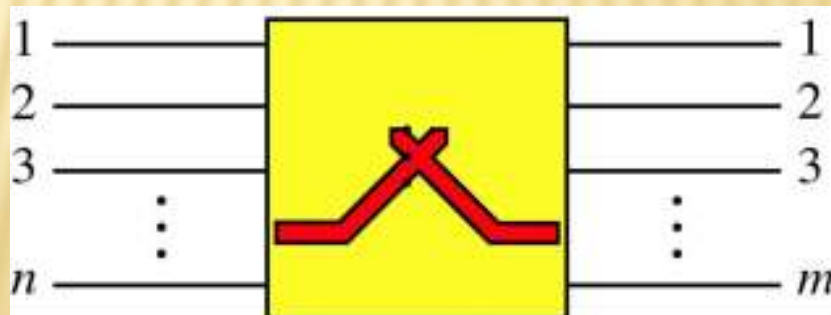
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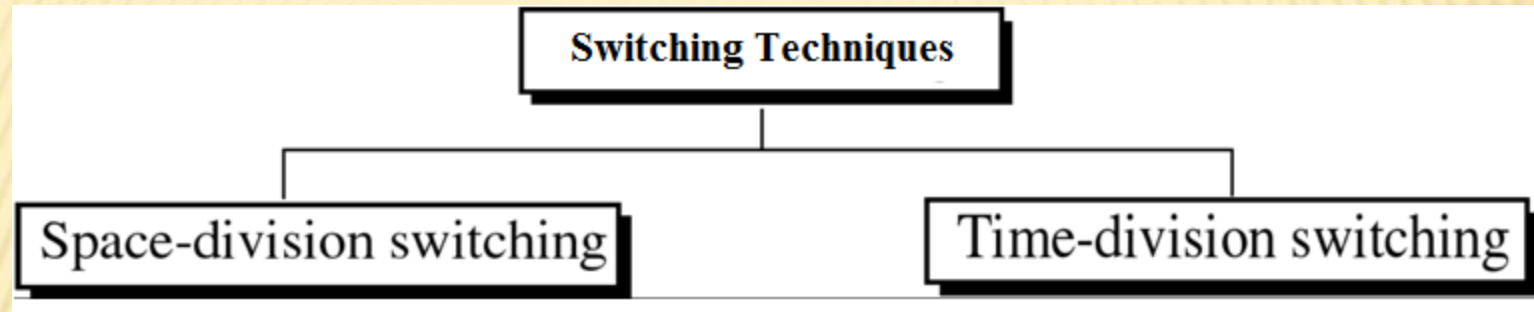


CIRCUIT-SWITCHED NETWORK



Switch





Space-division switching : paths in the circuit are separated from each other spatially.

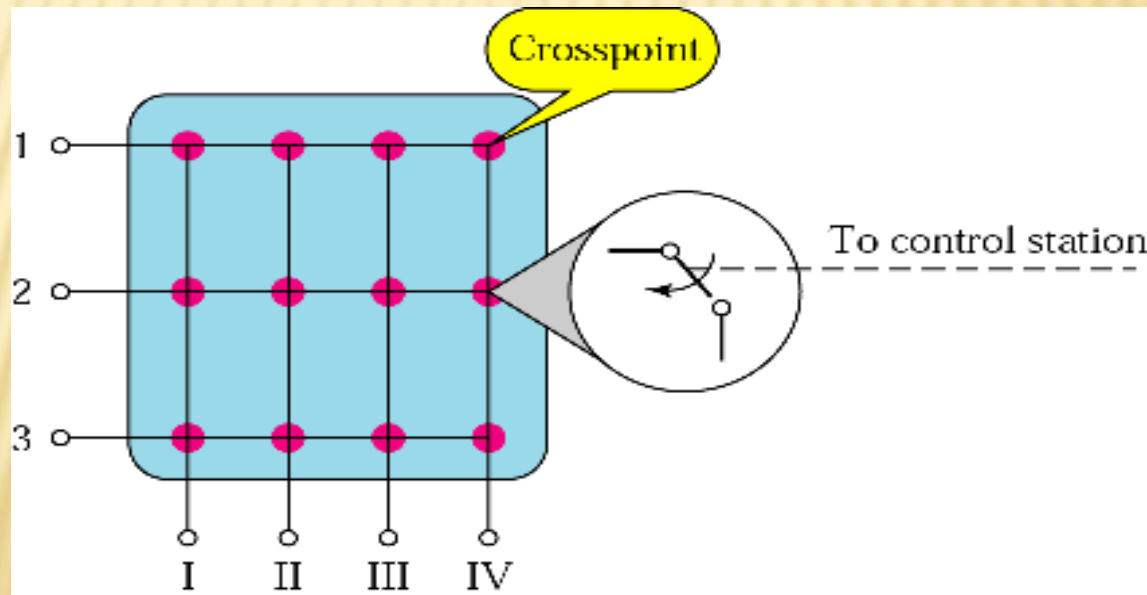
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- TDM bus

SPACE DIVISION SWITCH

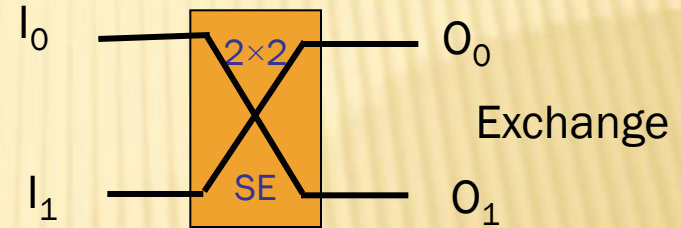
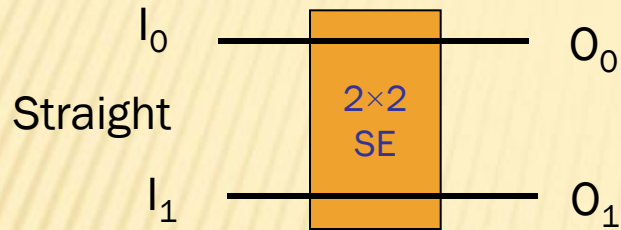
CROSSBAR SWITCH

- ❖ Crossbar switch connects n inputs to m outputs in a grid, using electronic micro-switches (transistors) at each cross-point.
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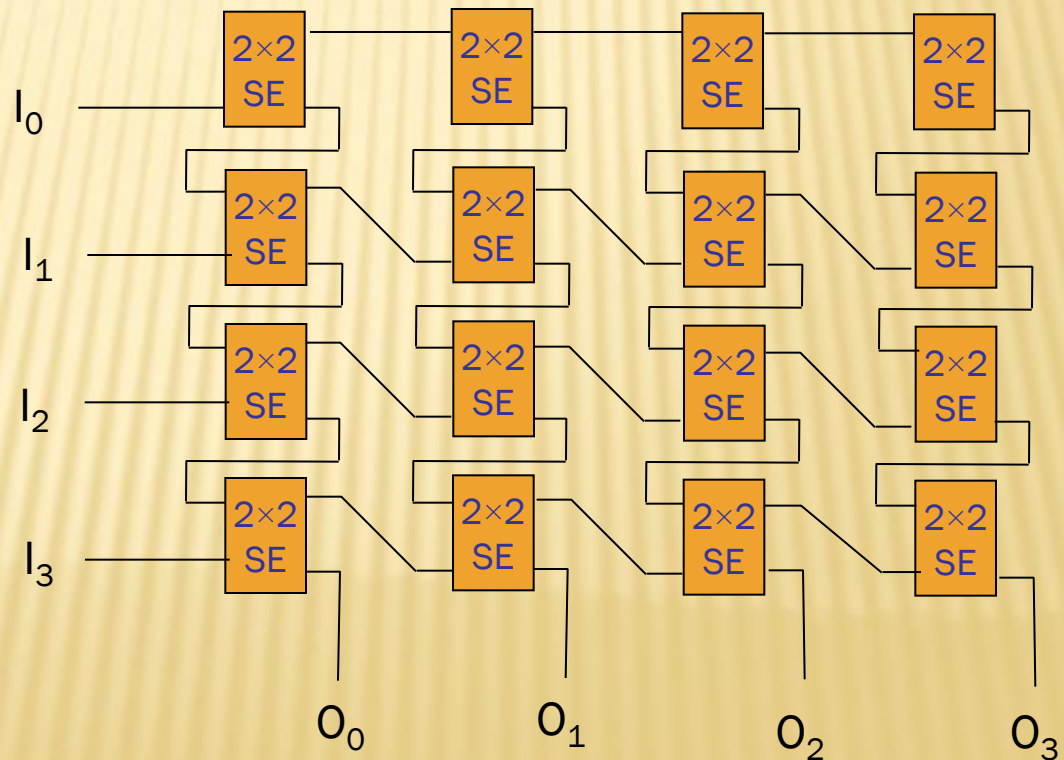


CROSSBAR IMPLEMENTATION

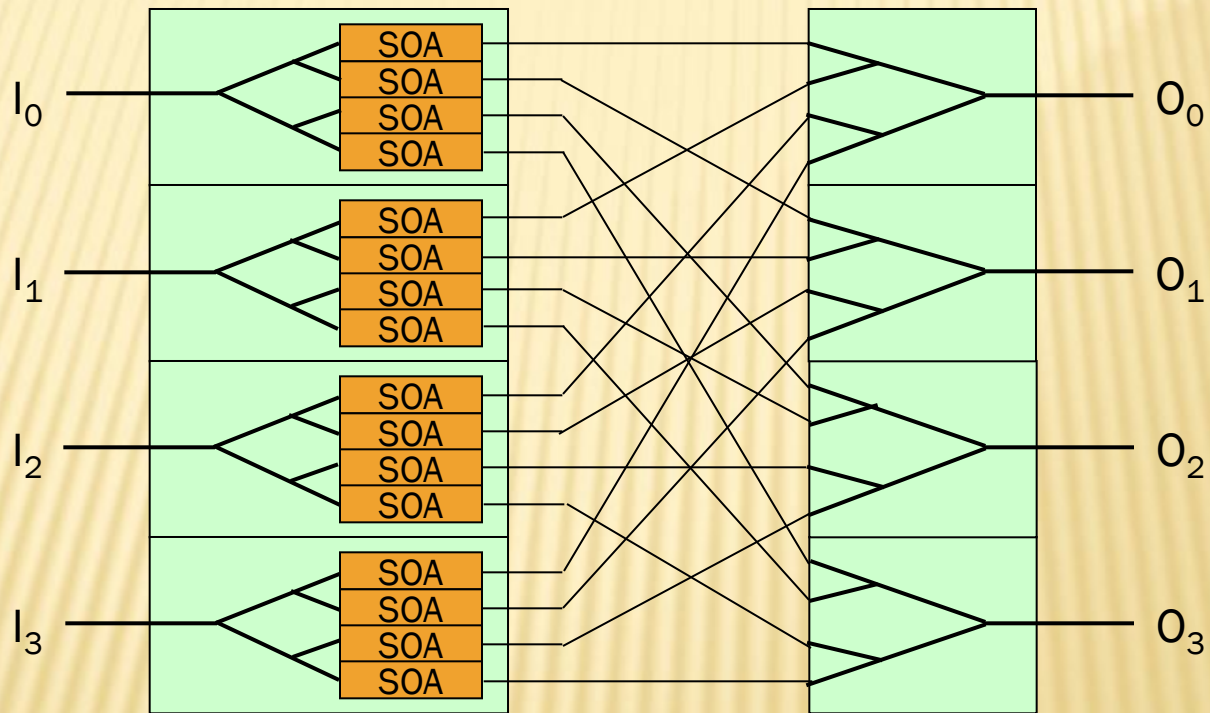
2×2 Switching element



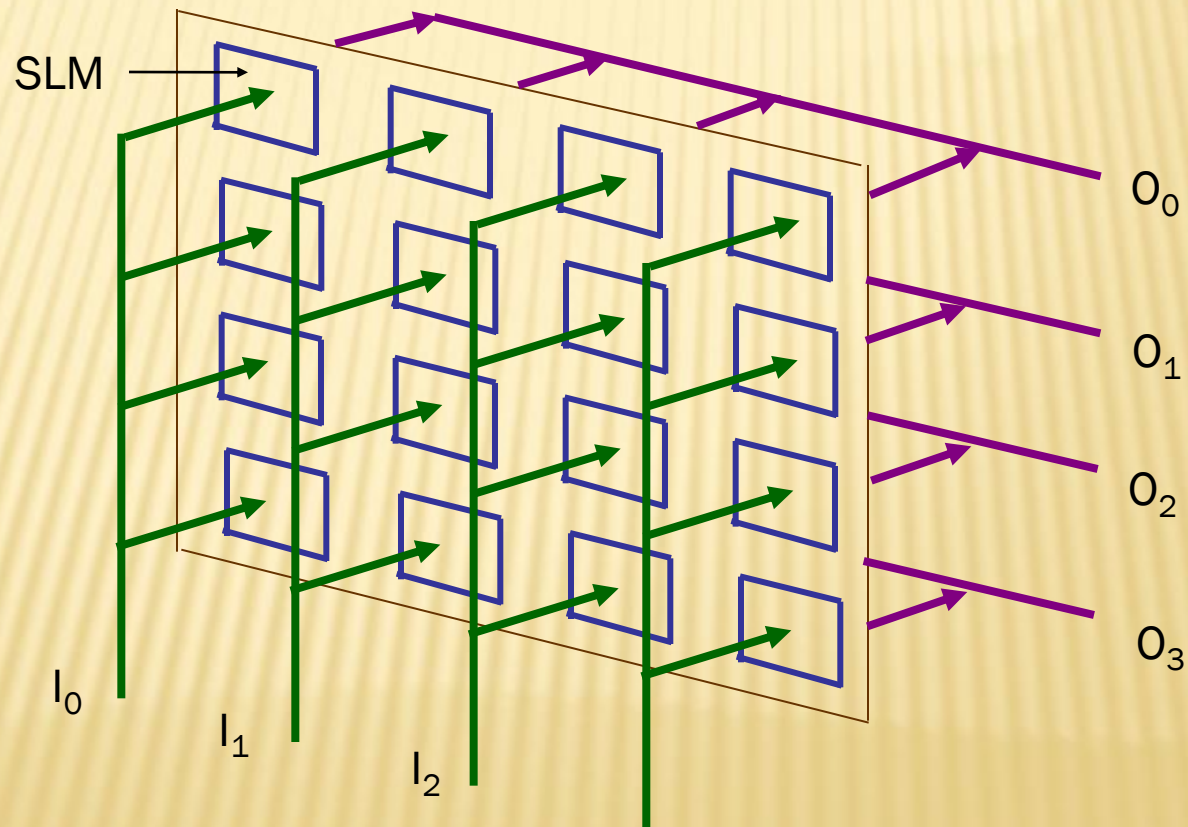
4×4 crossbar switch
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4×4 CROSSBAR SWITCH BASED ON SEMICONDUCTOR OPTICAL AMPLIFIER (SOA)

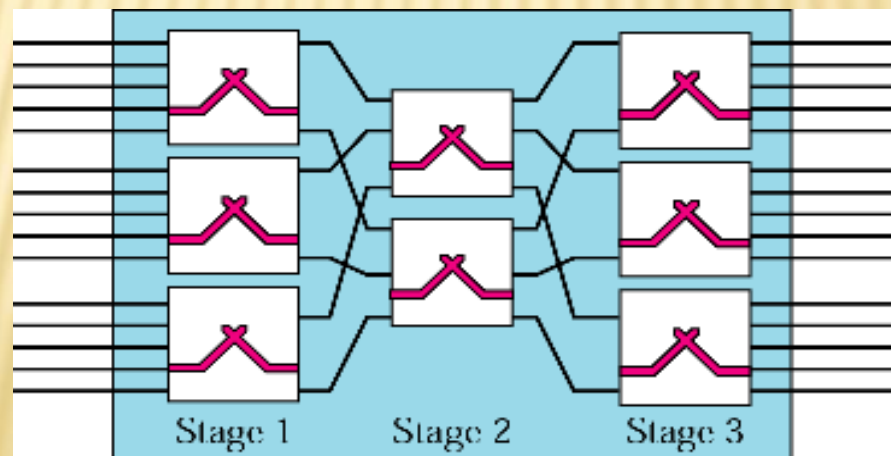


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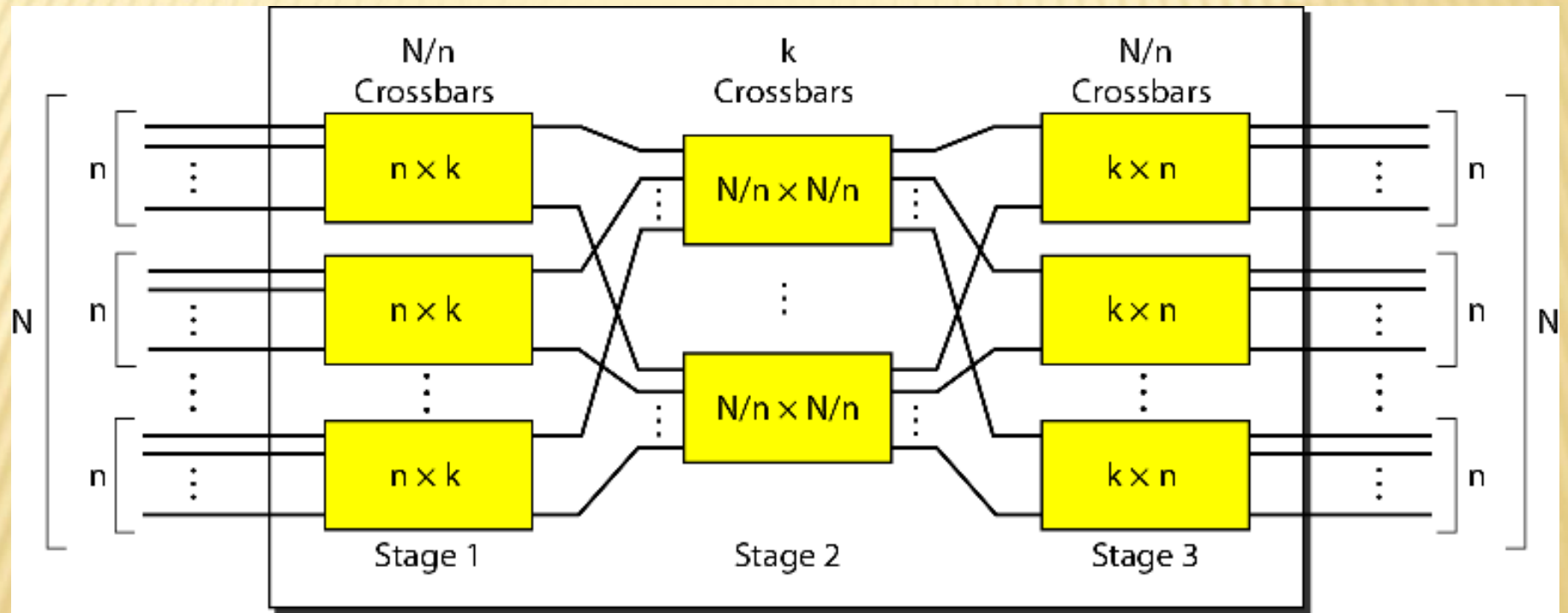


MULTISTAGE SWITCH

- ✗ Multistage switch combines crossbar switches in several stages.
- ✗ Design of a multistage switch depends on the number of stages and the number of switches required (or desired) in each stage.
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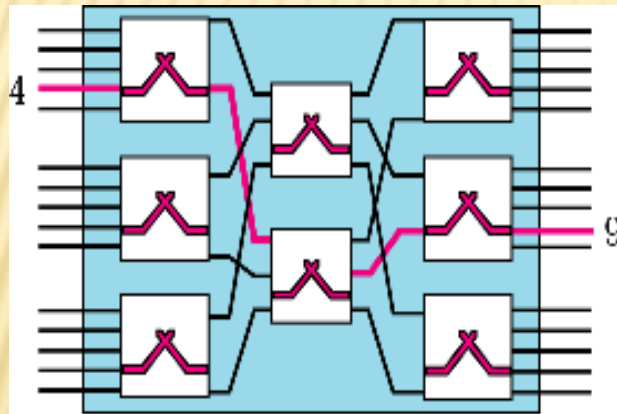


Multistage switch

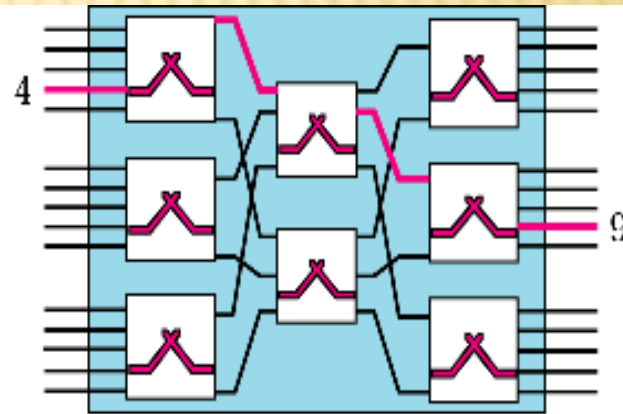


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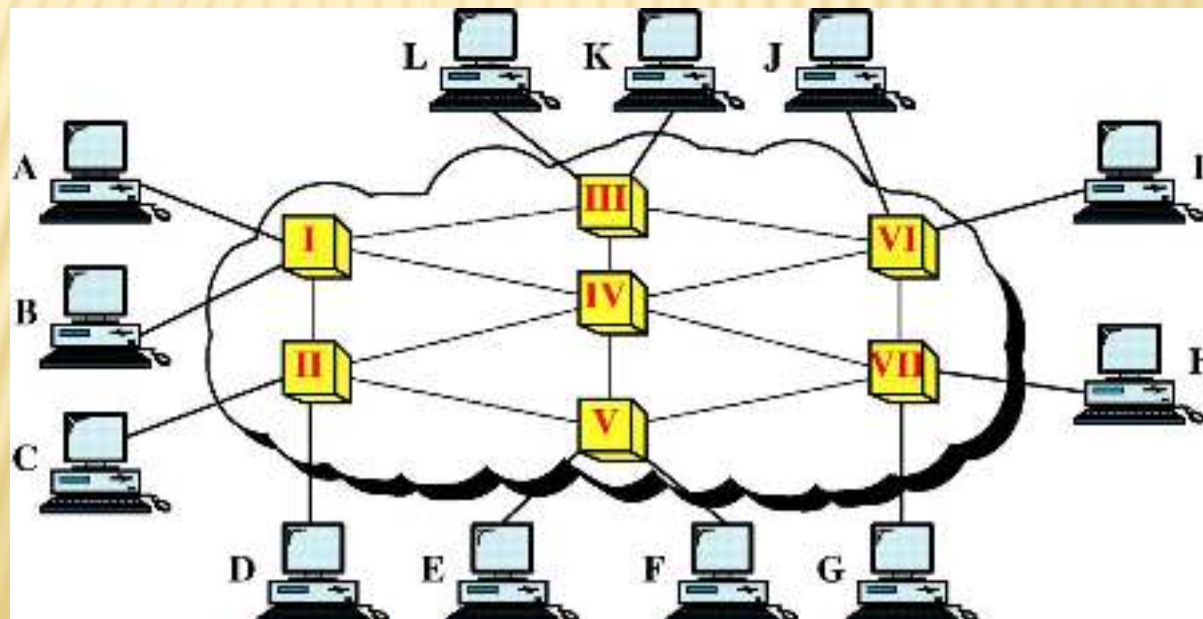


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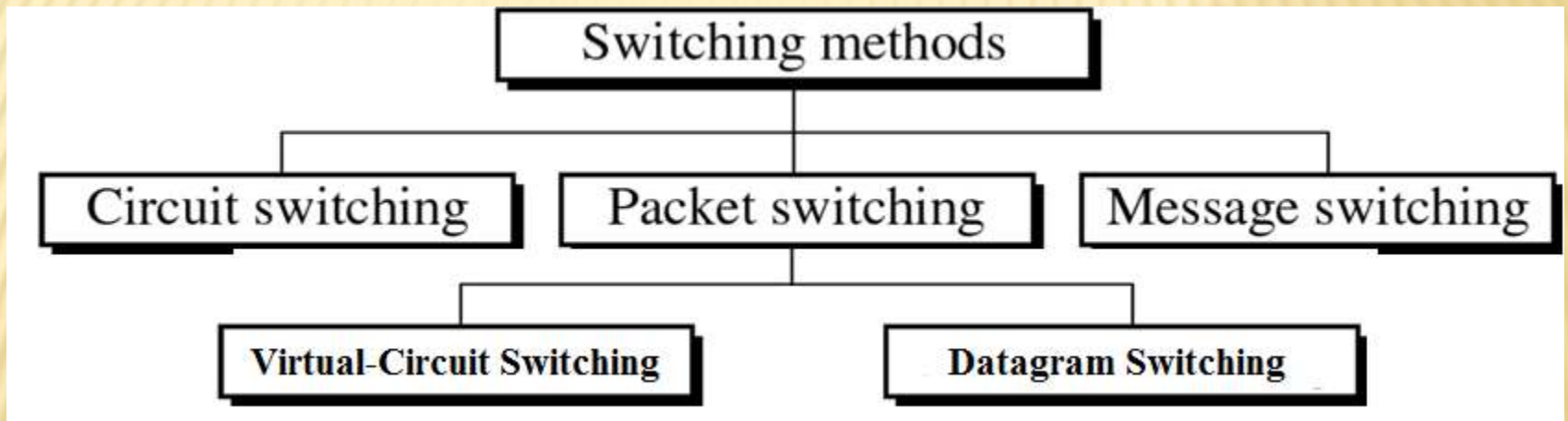
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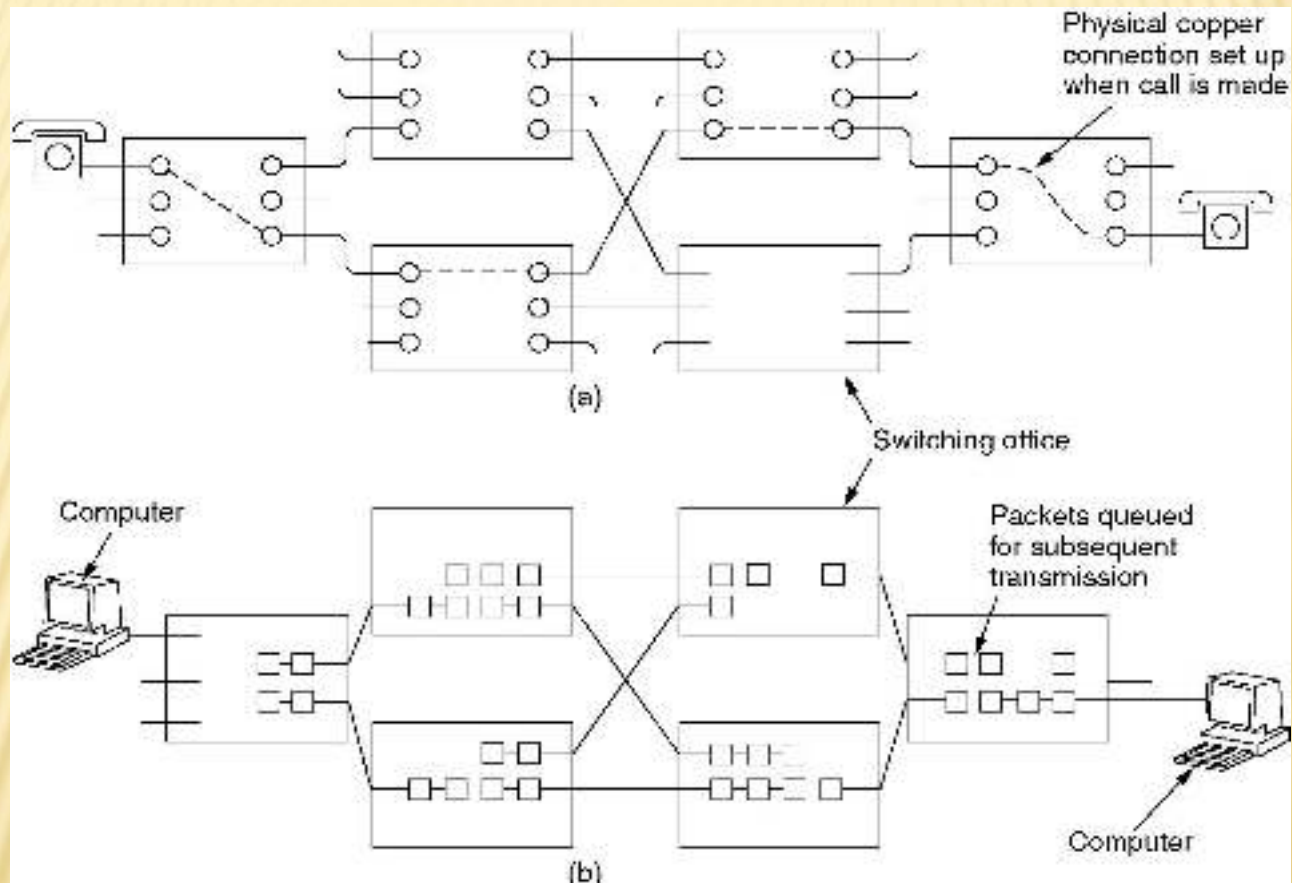
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(a) Circuit switching

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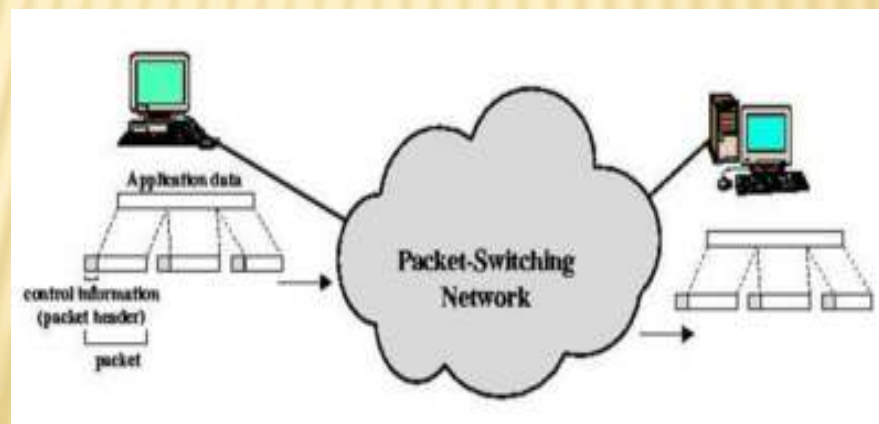
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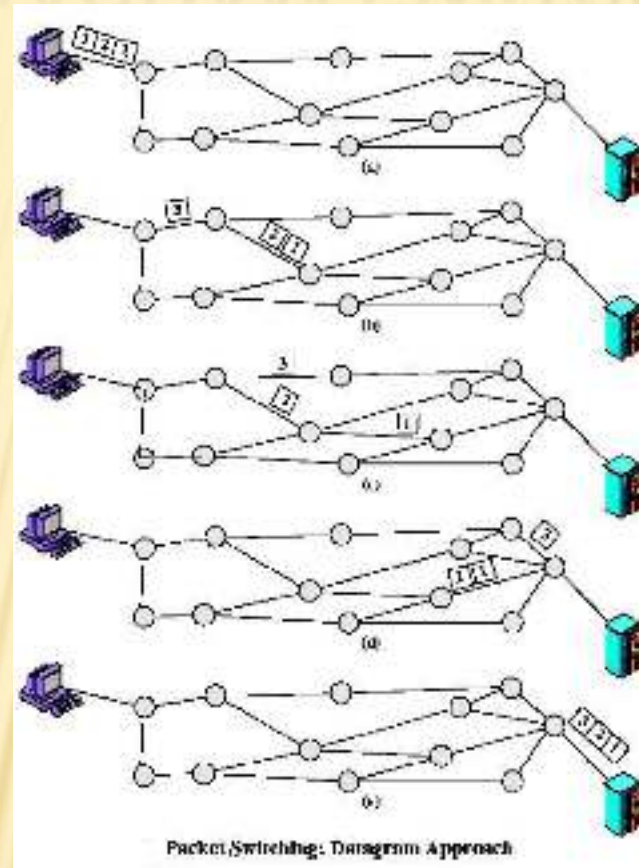
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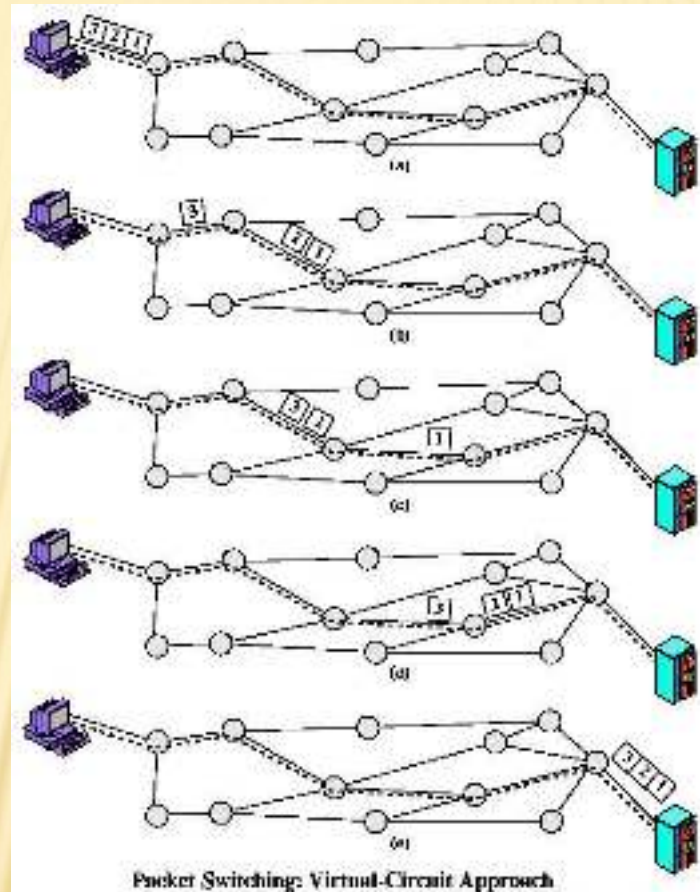
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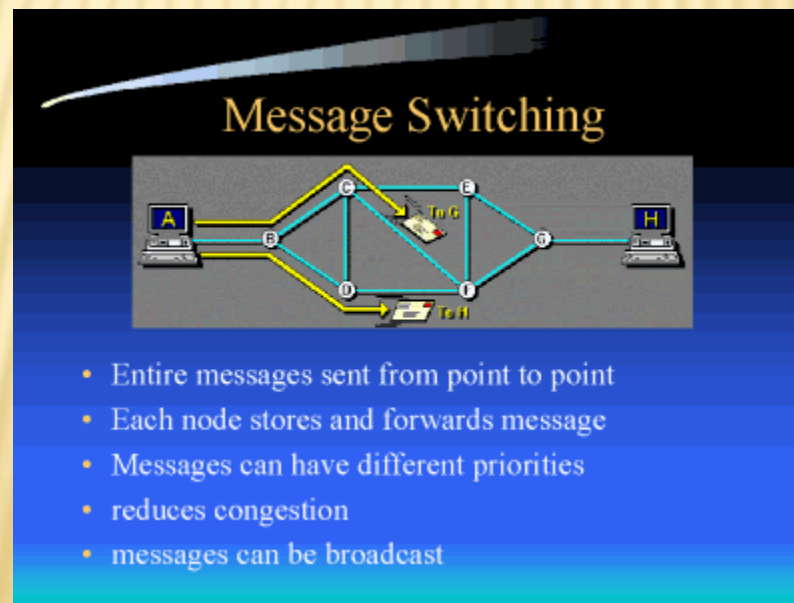
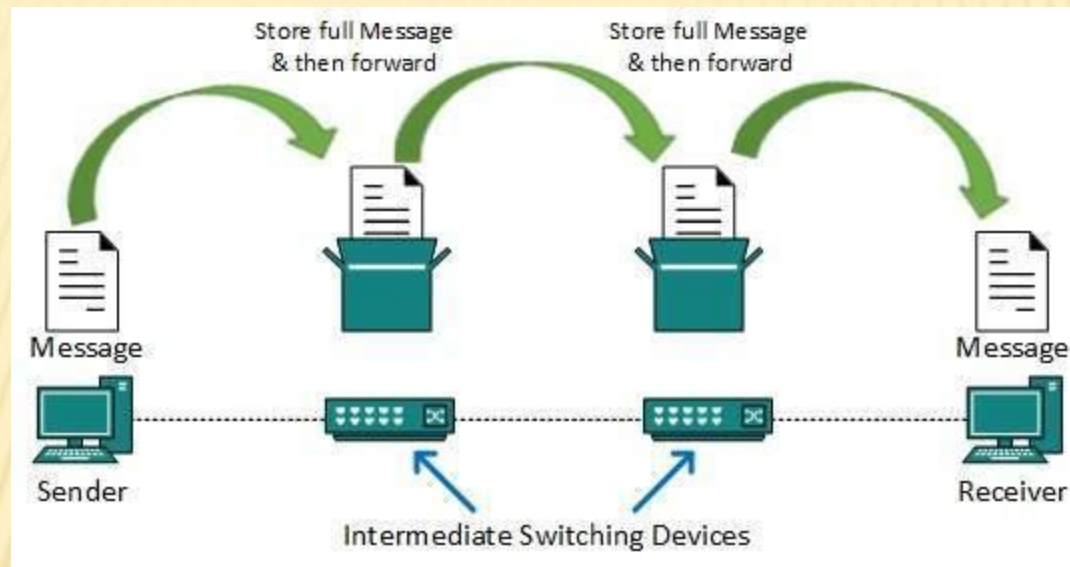
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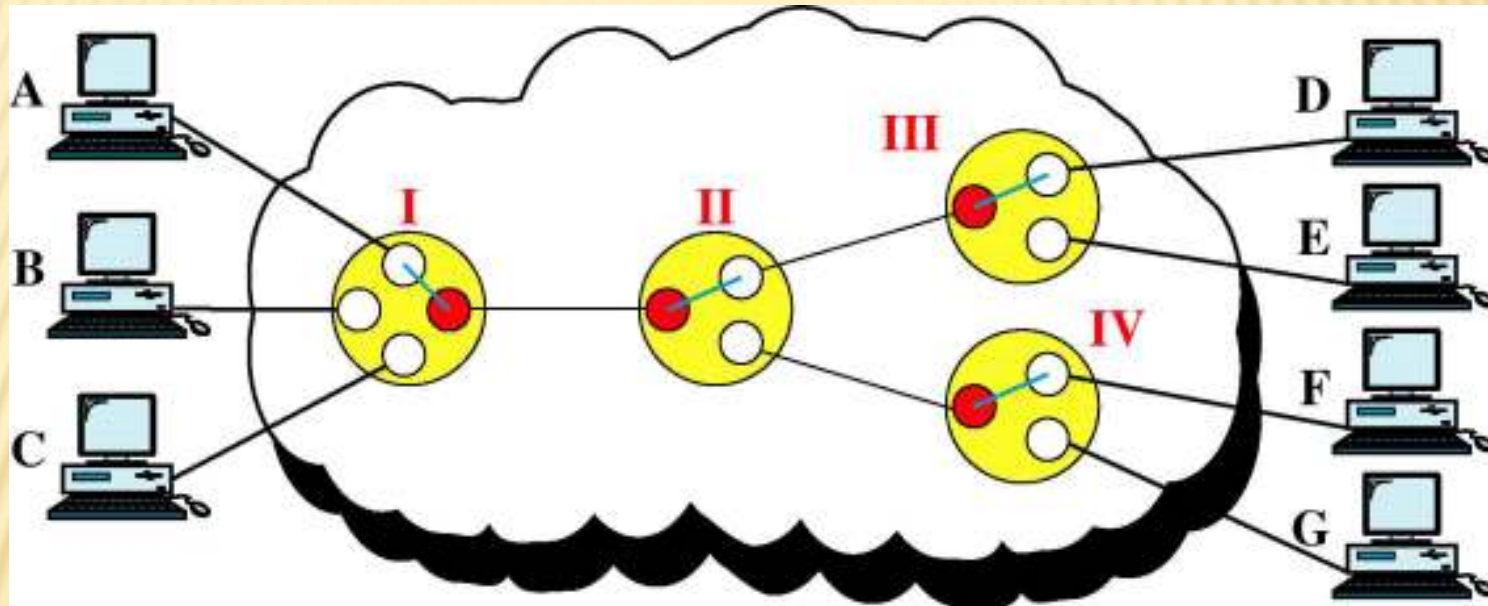
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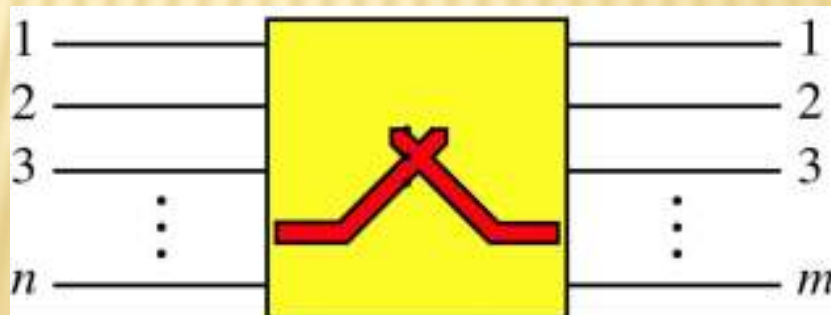
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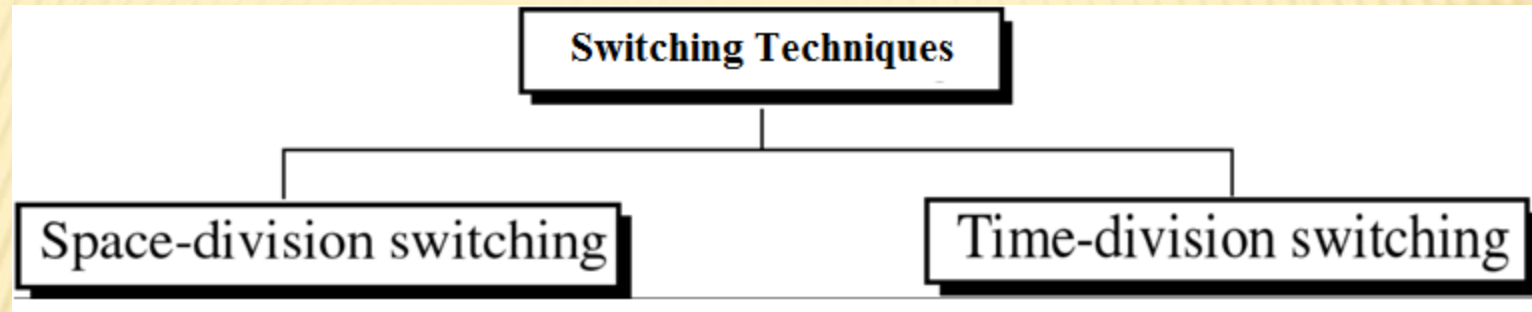


CIRCUIT-SWITCHED NETWORK



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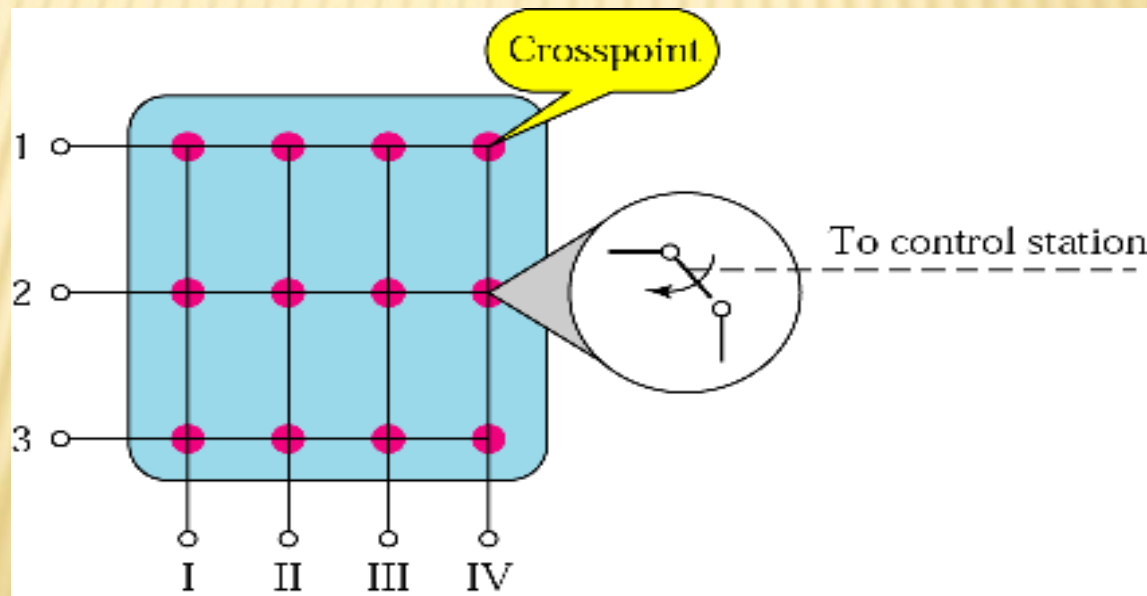
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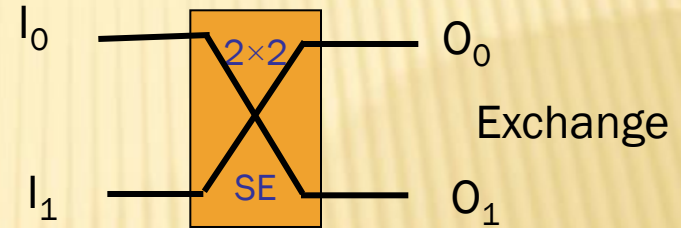
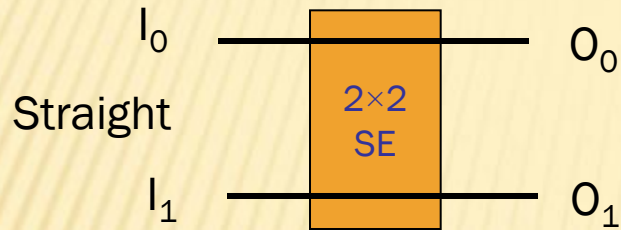
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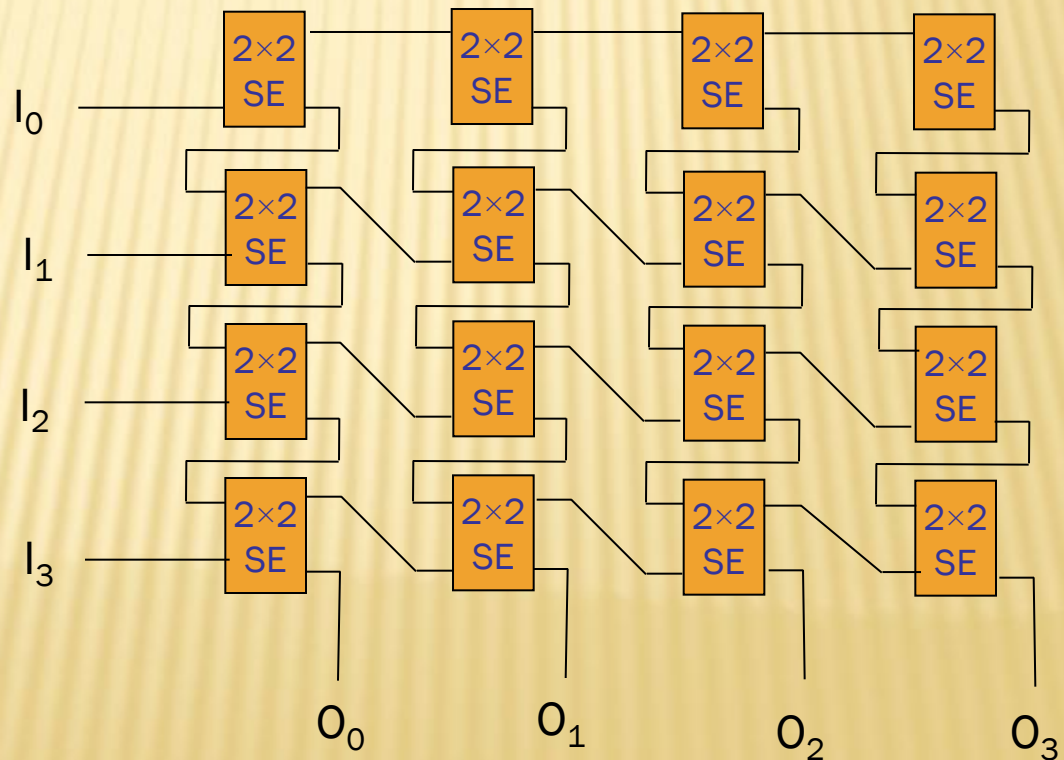


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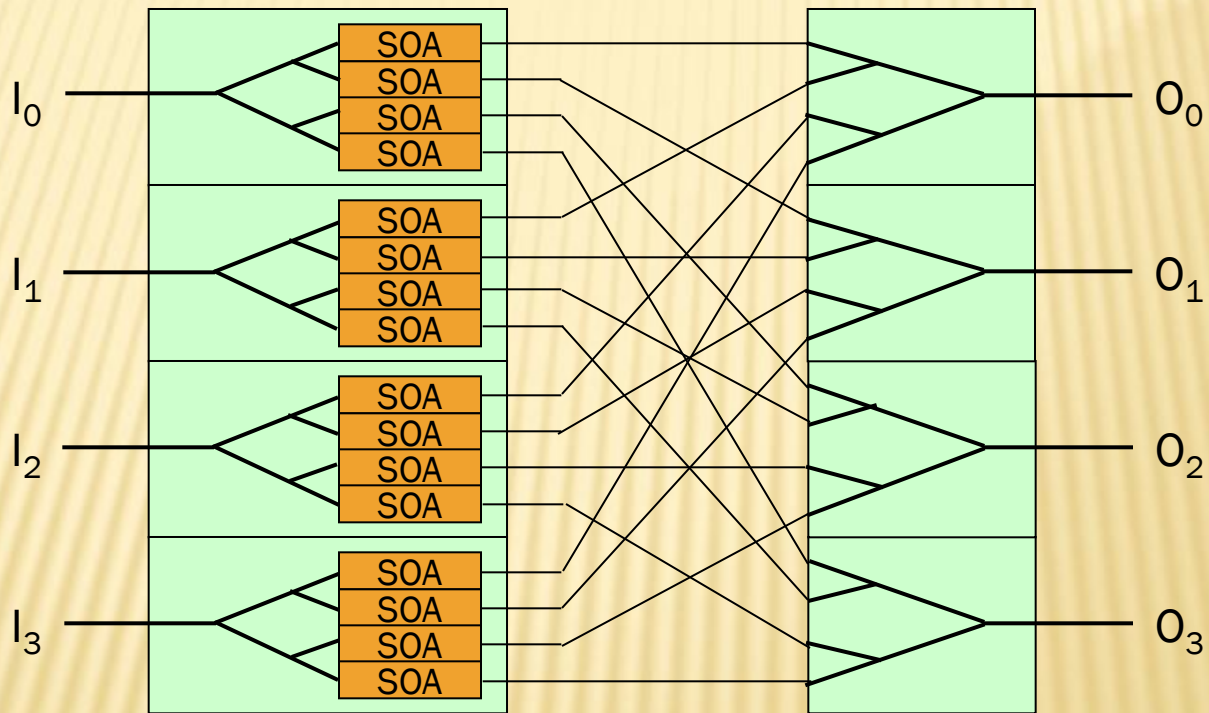
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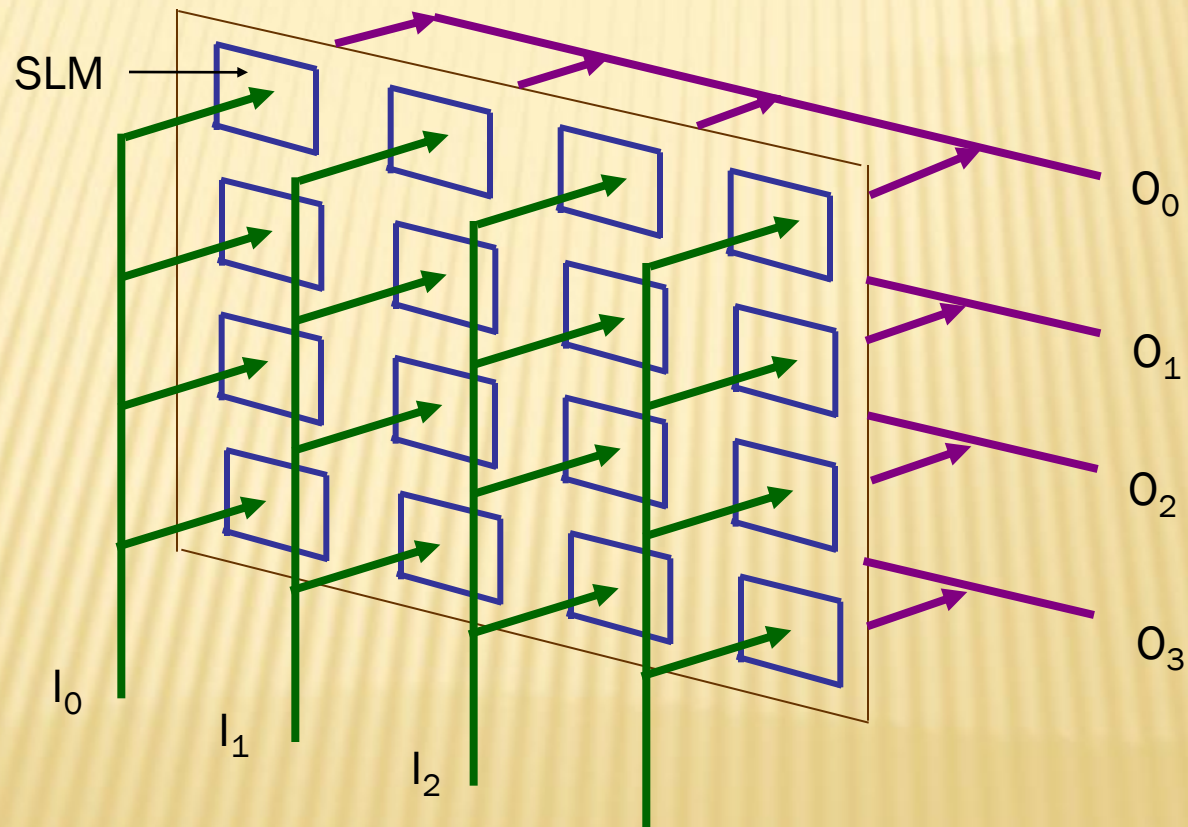
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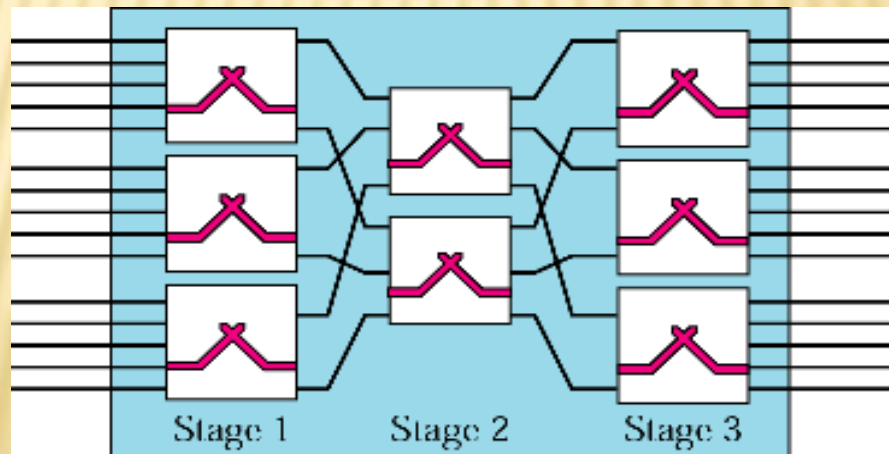


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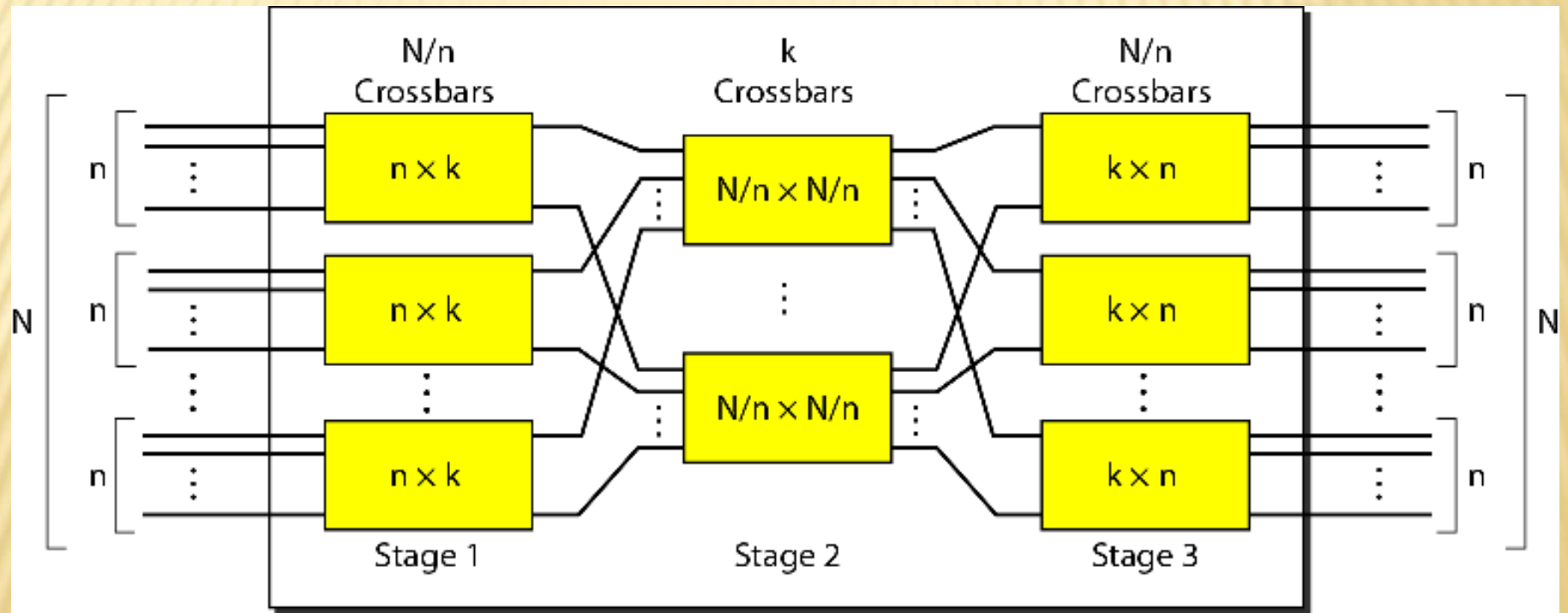


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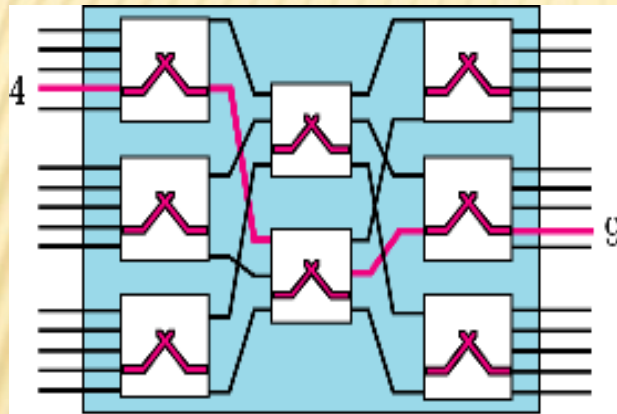


Multistage switch

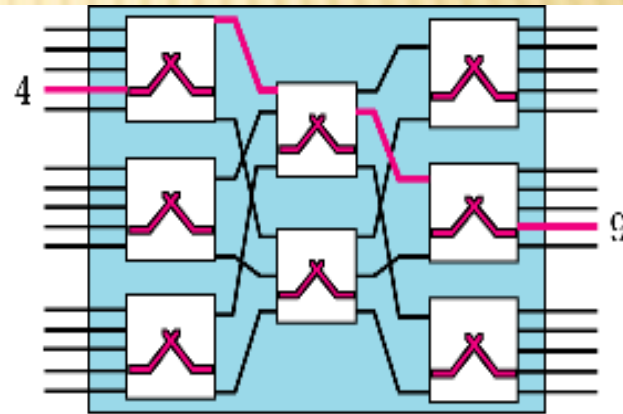


MULTIPLE SWITCHING PATHS

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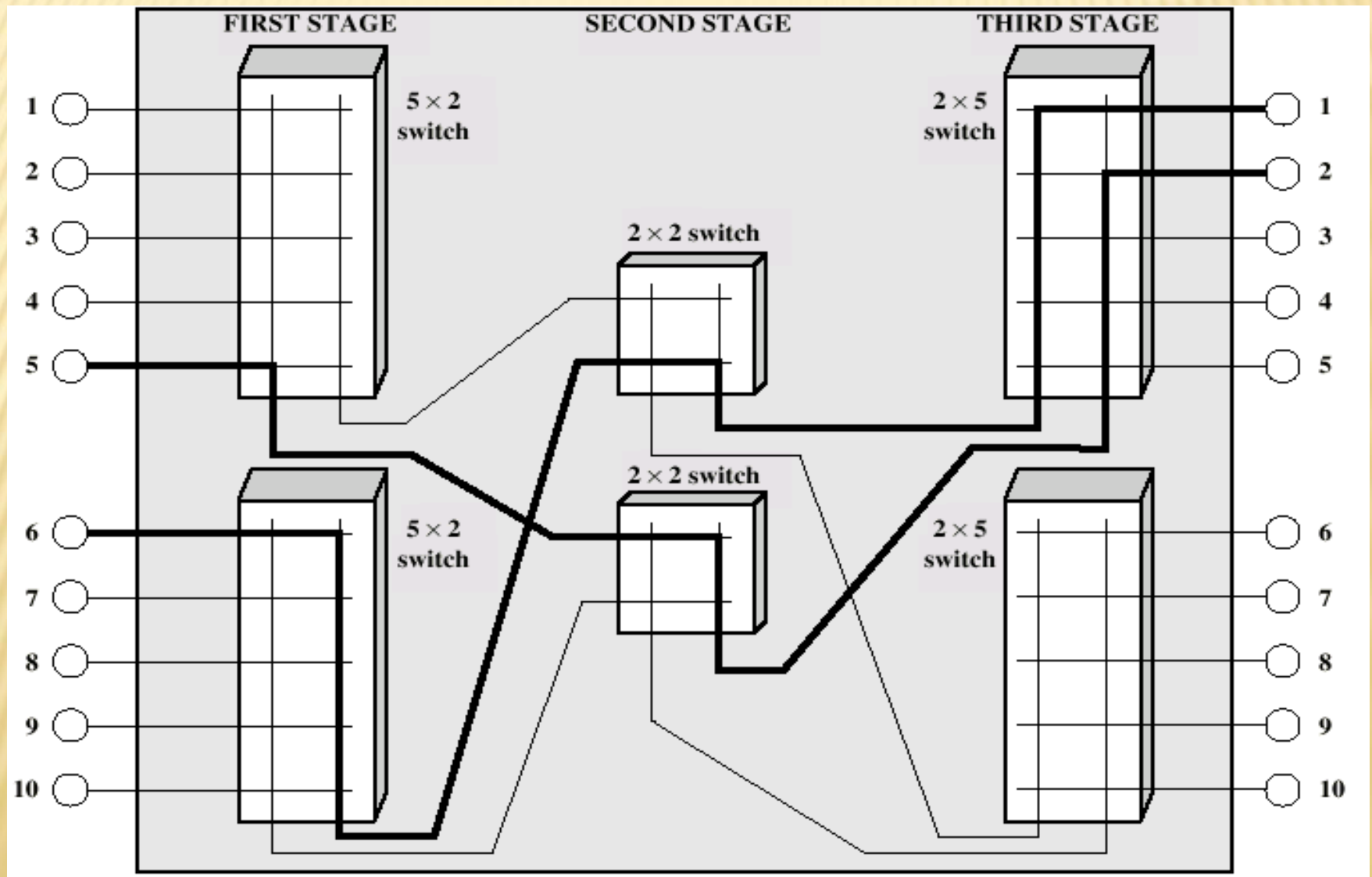


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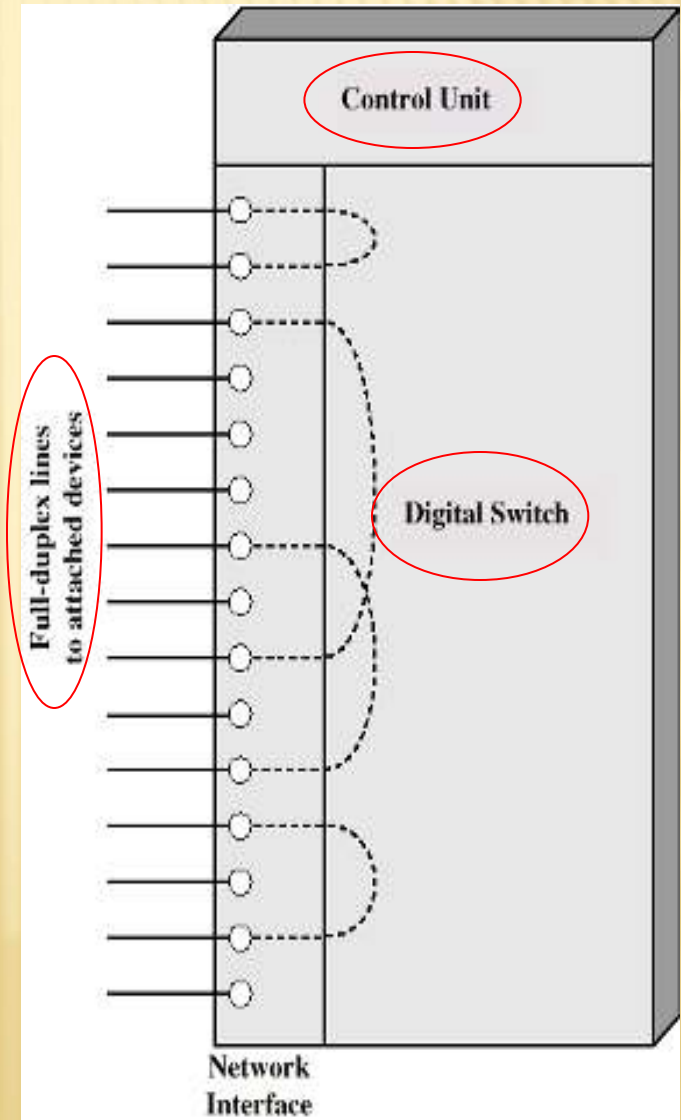
b. Second option

THREE STAGES SWITCH



CIRCUIT SWITCH CONCEPTS & ELEMENTS

- Digital Switch
 - Provide transparent signal path between devices
- Network Interface
- Control Unit
 - Establish connections
 - Generally on demand
 - Handle and acknowledge requests
 - Determine if destination is free
 - construct path
 - Maintain connection
 - Disconnect



DIGITAL SWITCH: BLOCKING VS. NON-BLOCKING

- **Blocking**

- A network is unable to connect end stations because all paths are in use
- Used on voice systems
 - Short duration calls

- **Non-blocking**

- Permits all stations to connect (in pairs) at once
- Used for some data connections

II. Multistage Interconnection Networks (MINs):

Characteristics:

1. Full Access:

- ❖ Every input link can reach to any output link in a single pass.
- ❖ In MINs, by using 2×2 switching elements, only $\log_2 N$ stages are required to achieve *full access capability*.

2. Strictly Non-Blocking vs. Internal Blocking:

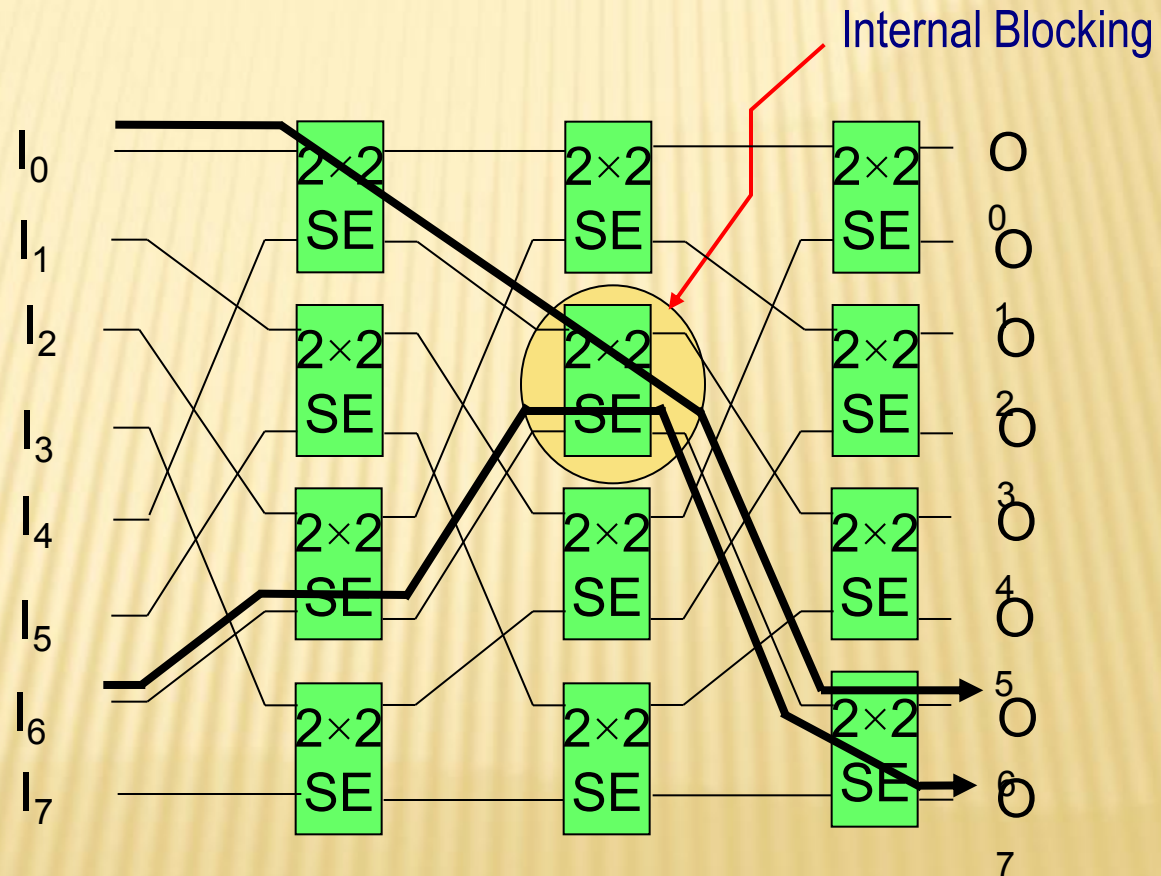
- ❖ **Strictly non-blocking Switch** can realize $N!$ permutations without any rearrangement of the existing connections.
- ❖ MINs with fewer stages suffer problem **of internal blocking**.

INTERNAL BLOCKING IN (MIN)

Internal Blocking
occurs for the
connections:

0 → 6

6 → 7



3. Rearrangeable Networks:

- ❖ MINs are capable to realize $N!$ permutations by choosing the appropriate connections.
- ❖ This type of MINs requires a large number of stages ($3\log_2 N - 4$).

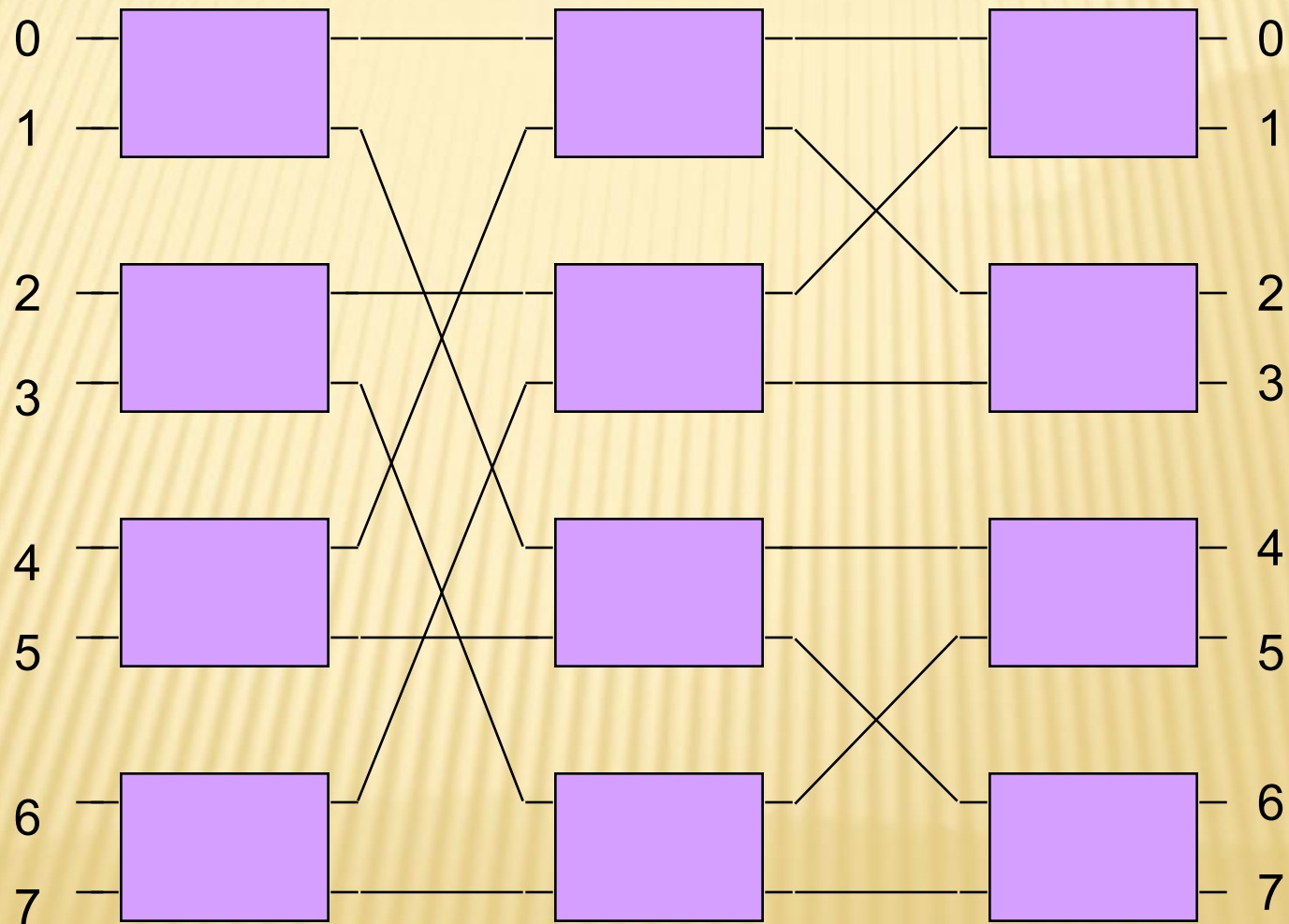
4. Combinatorial Power:

- ❖ It is the ratio of the number of permutations realizable by the MINs to the total number of possible permutations ($N!$).
- ❖ A MIN has $\log_2 N$ stages are required to achieve full access capability, and in each stage, there are $N/2$ of 2×2 switching elements.
- ❖ Since each switching element has two configurations, namely straight and exchange, therefore, number of permutations realizable by the MINs is $2^{N/2 \cdot \log_2 N}$.

DELTA NETWORK

- The delta network is one example of a multistage interconnection network (Banyan Network) that can be used as a switch fabric.
- In banyan networks, there is a single path from each input port to each output port.

8 X 8 DELTA NETWORK



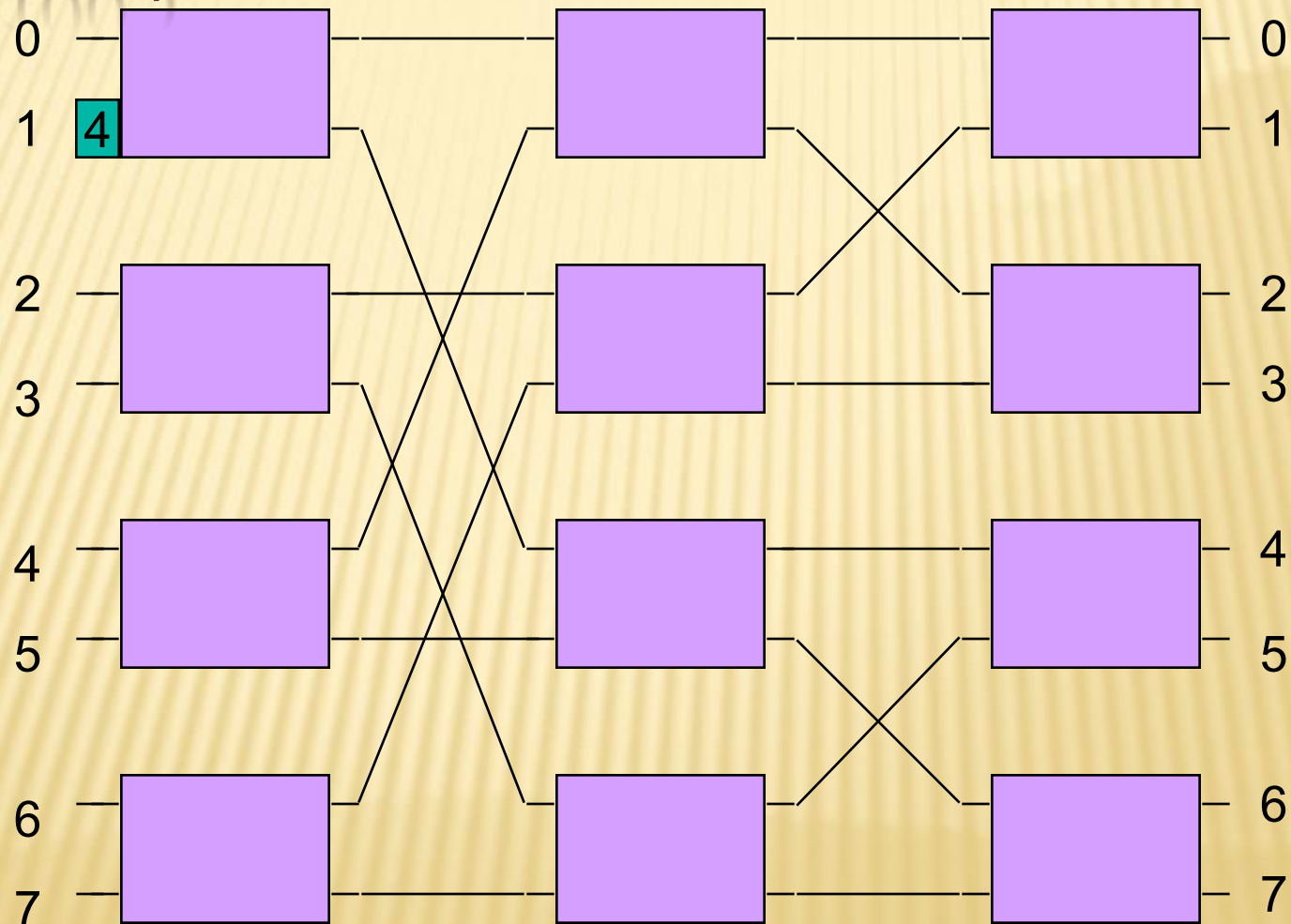
SELF ROUTING

- Delta network has self-routing property
- The path for a cell to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port

EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

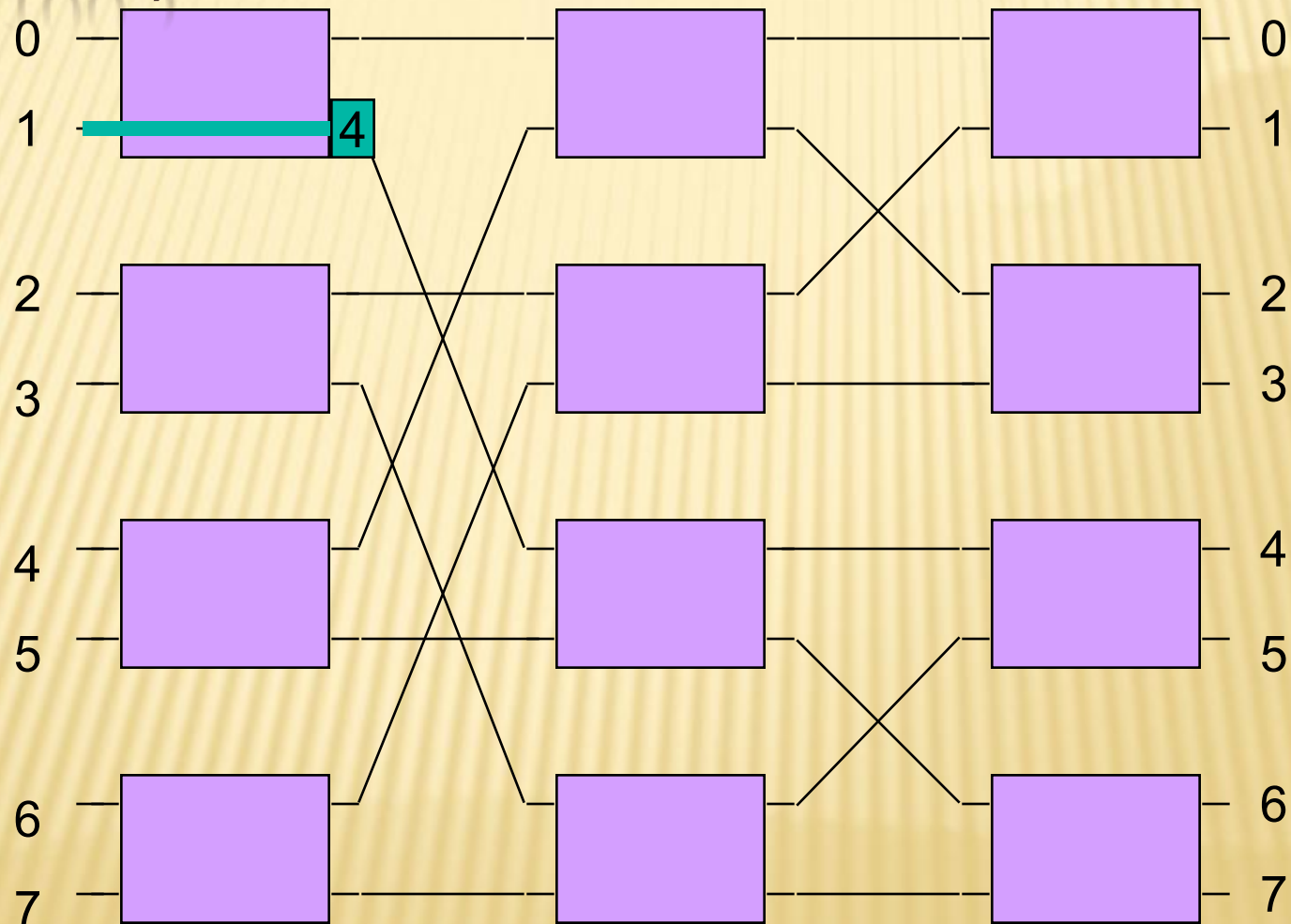
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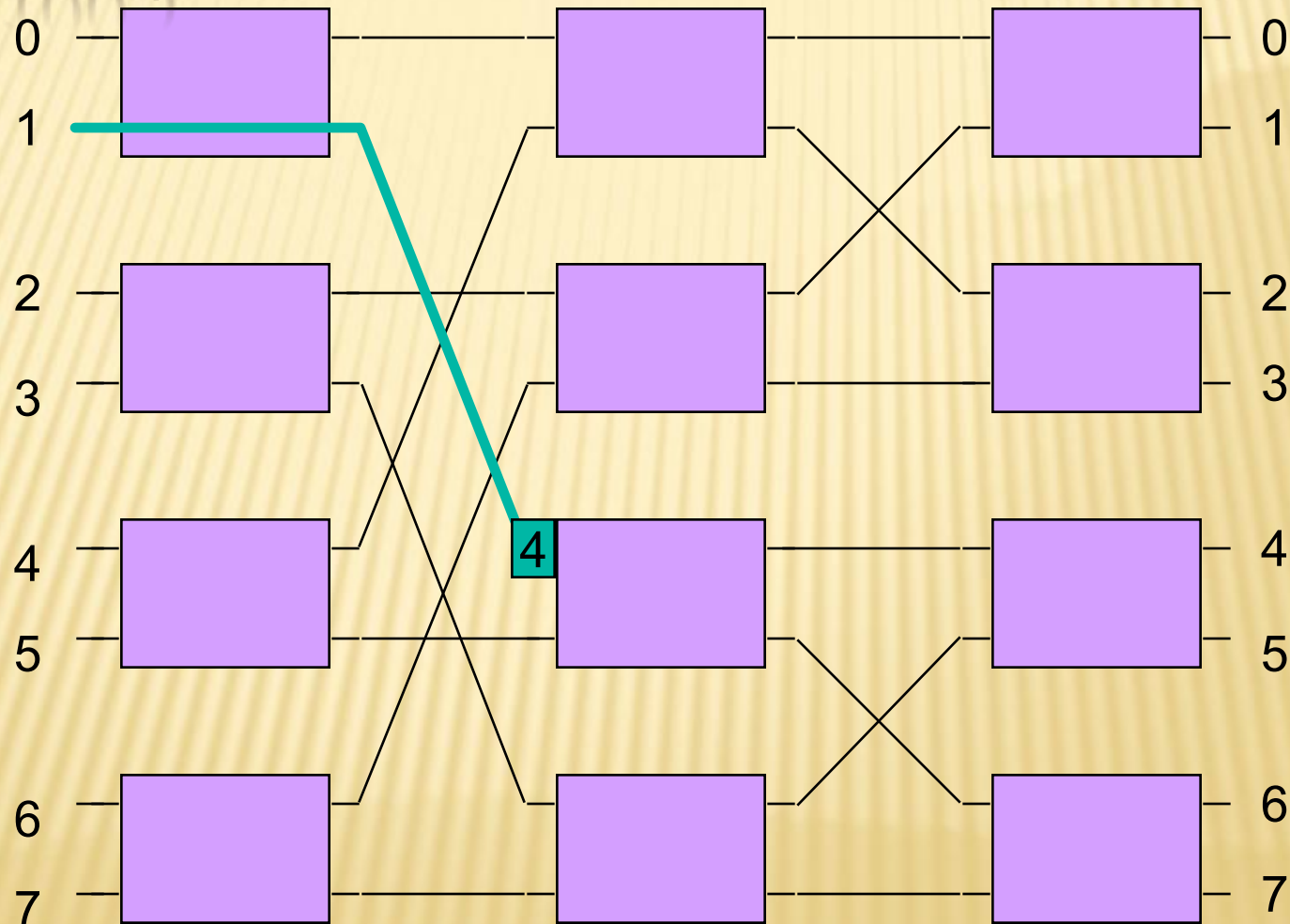
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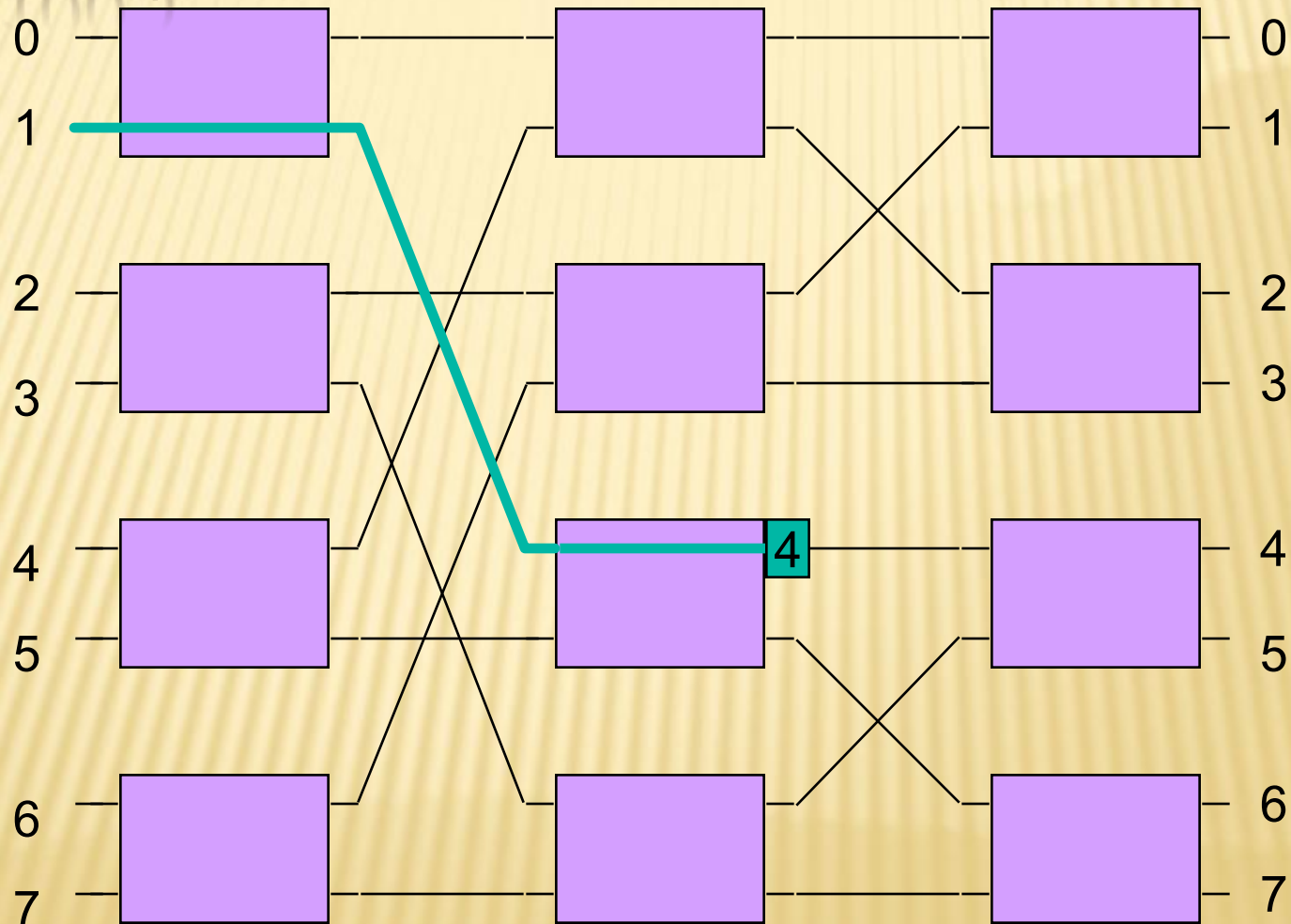
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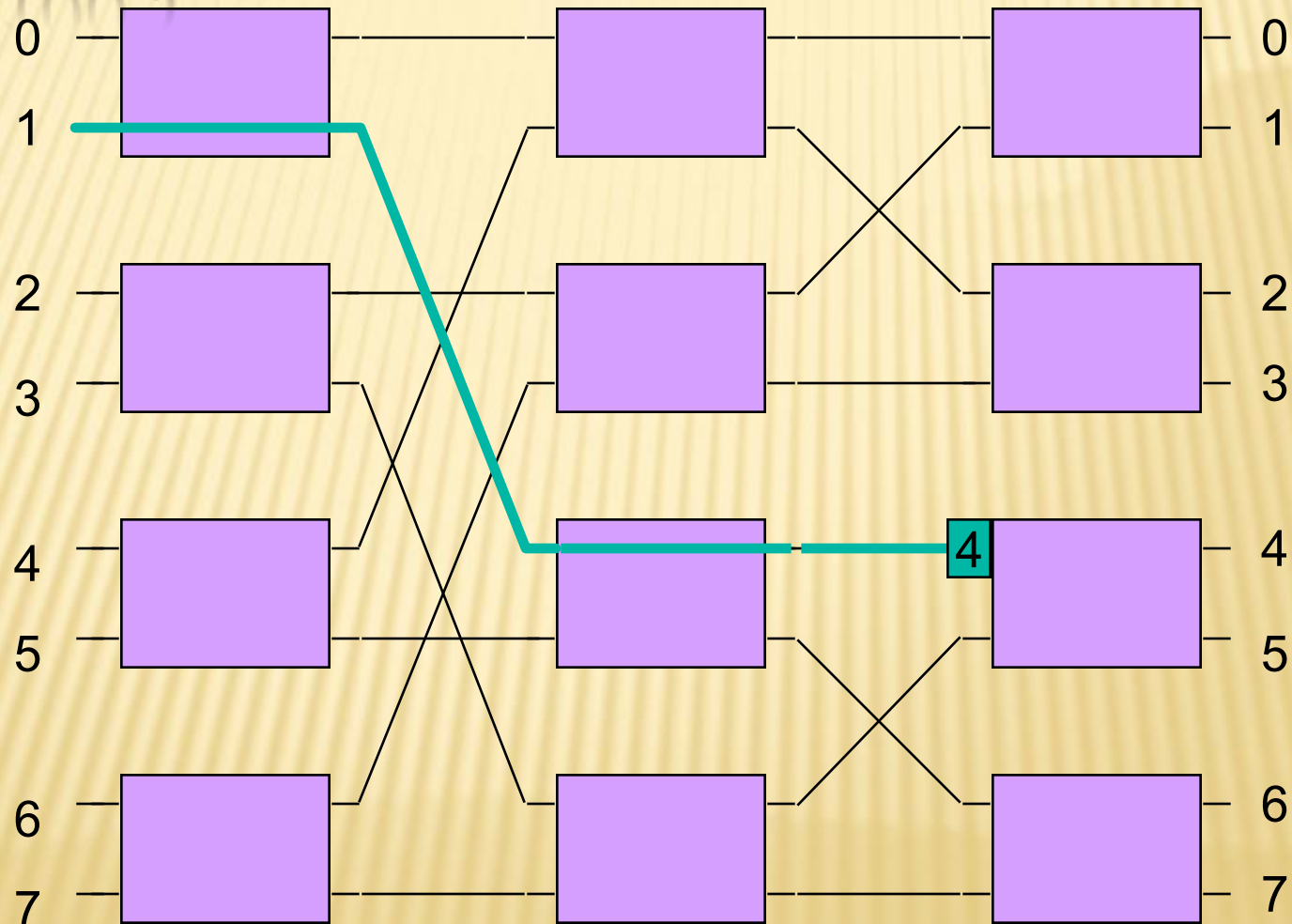
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2



EXAMPLE OF SELF ROUTING CELL DESTINED FOR OUTPUT PORT 4 (= 100)

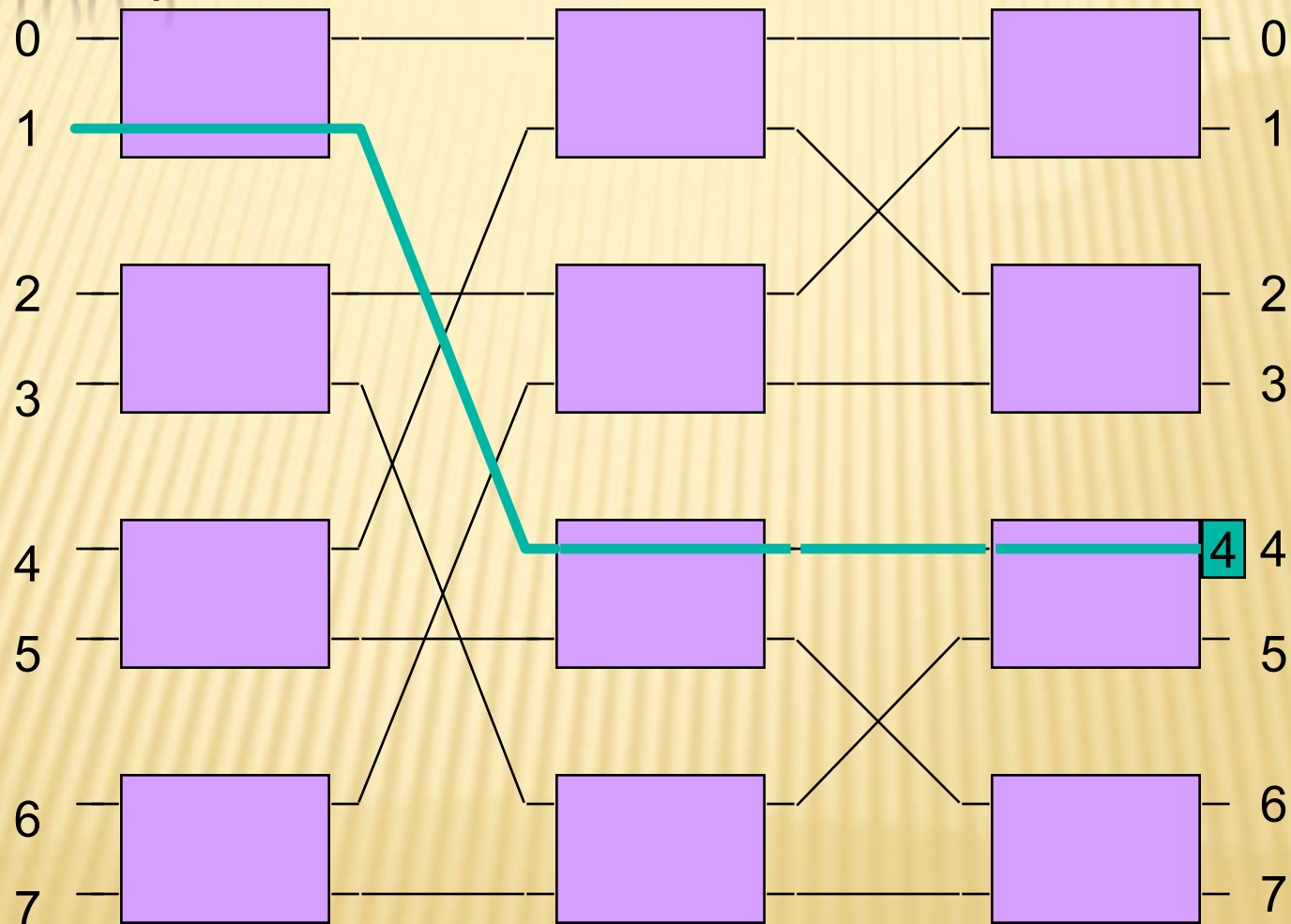
2



EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

2

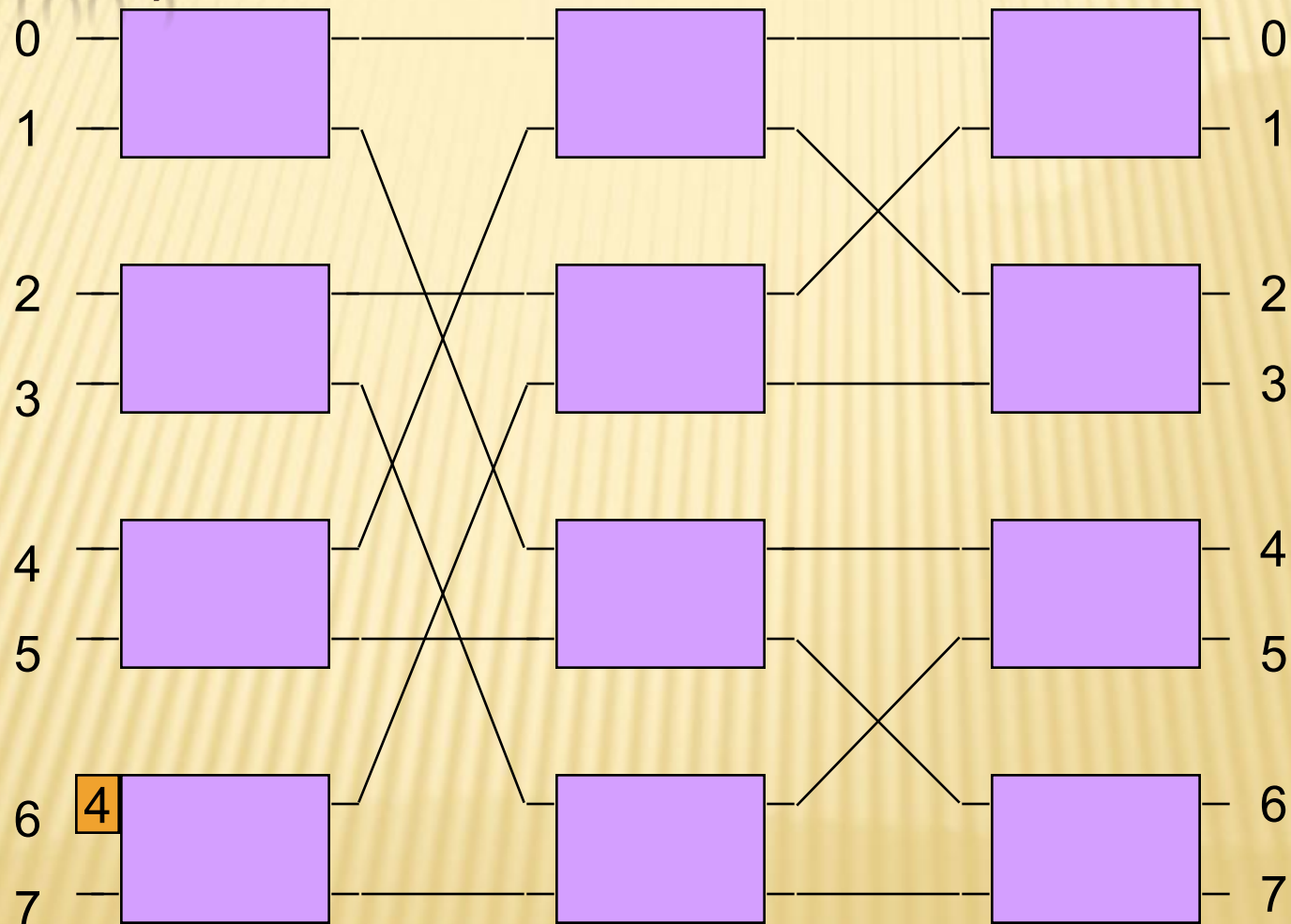


EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4

(= 100)

2

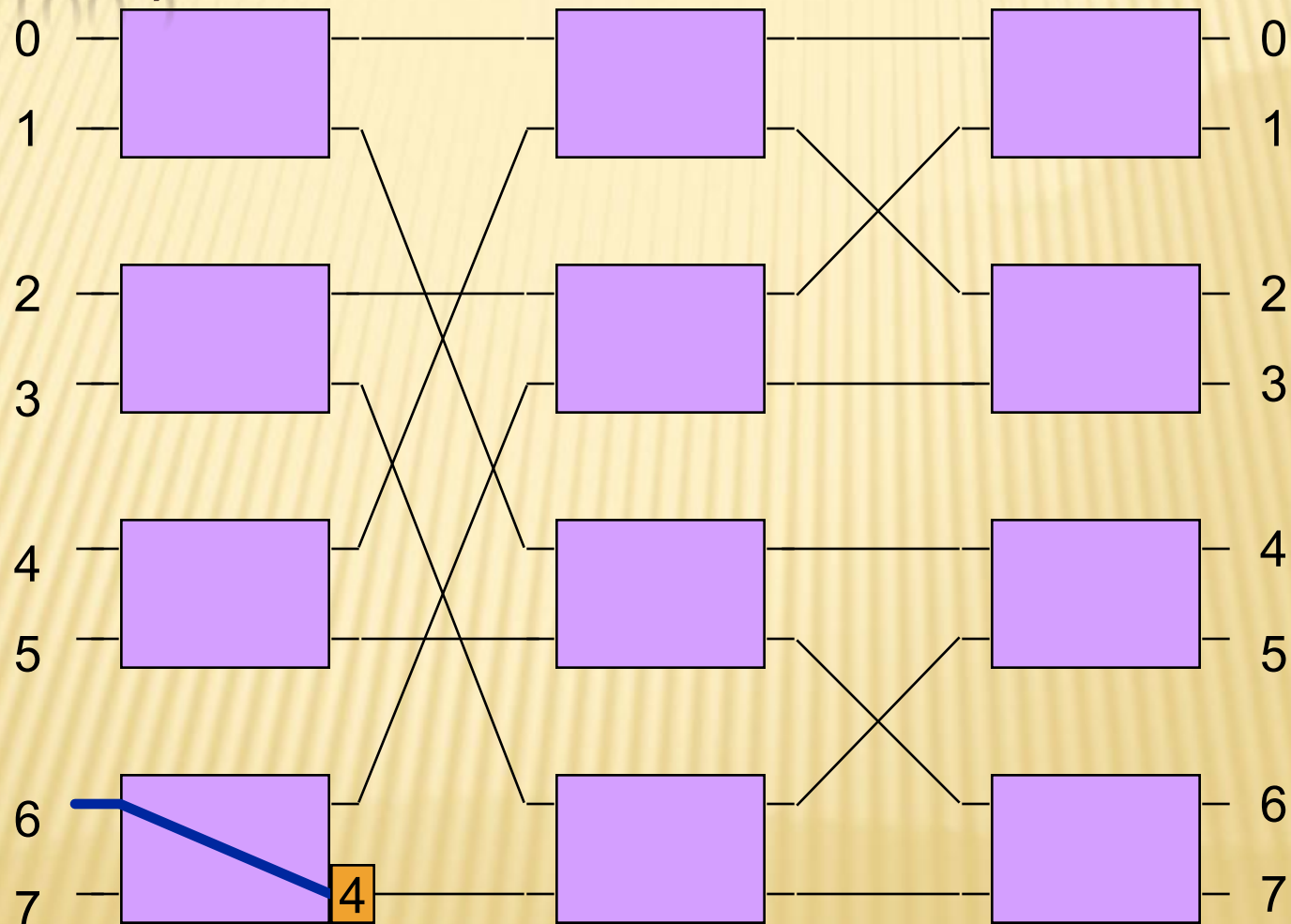


EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4

(= 100)

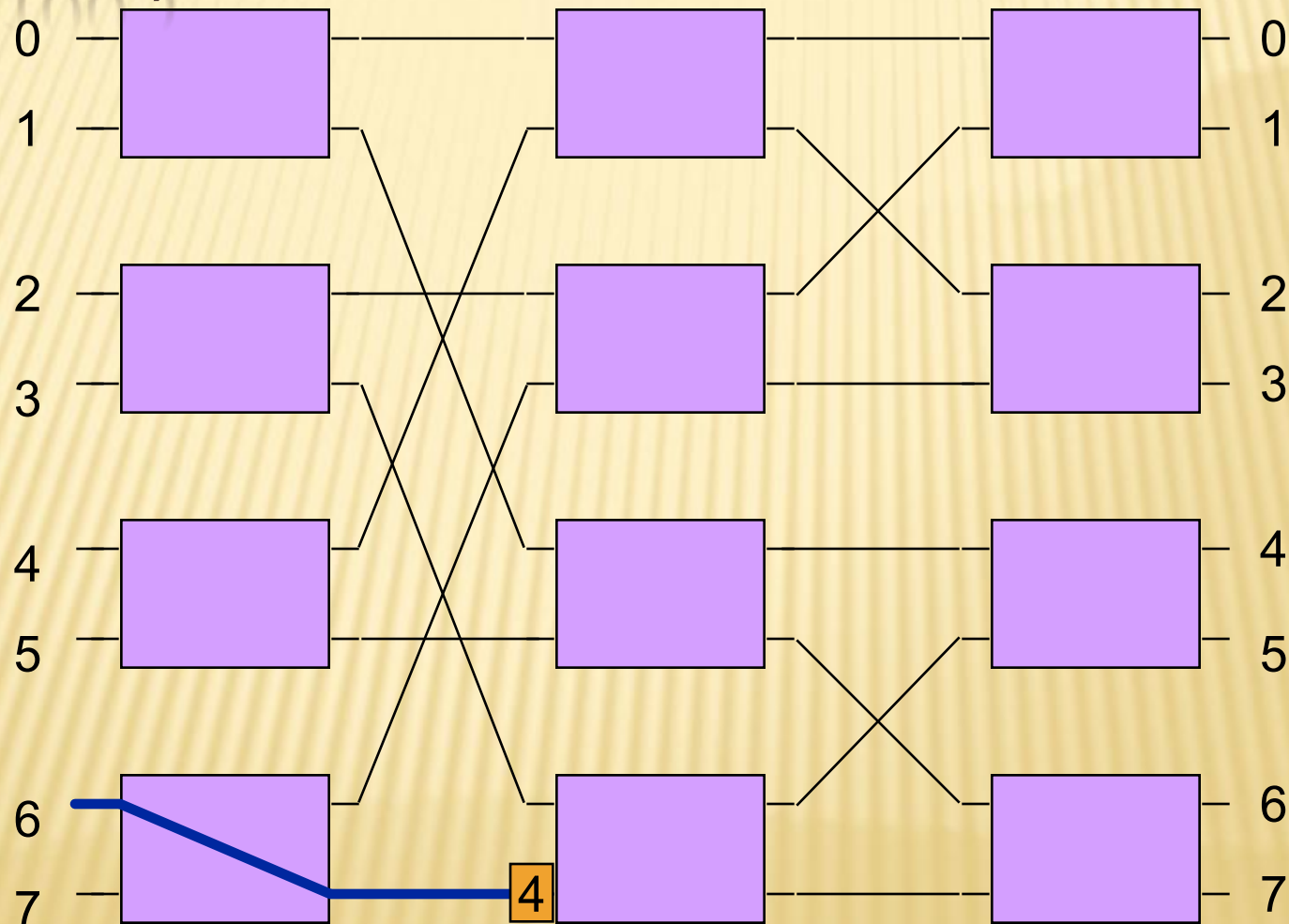
2



EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

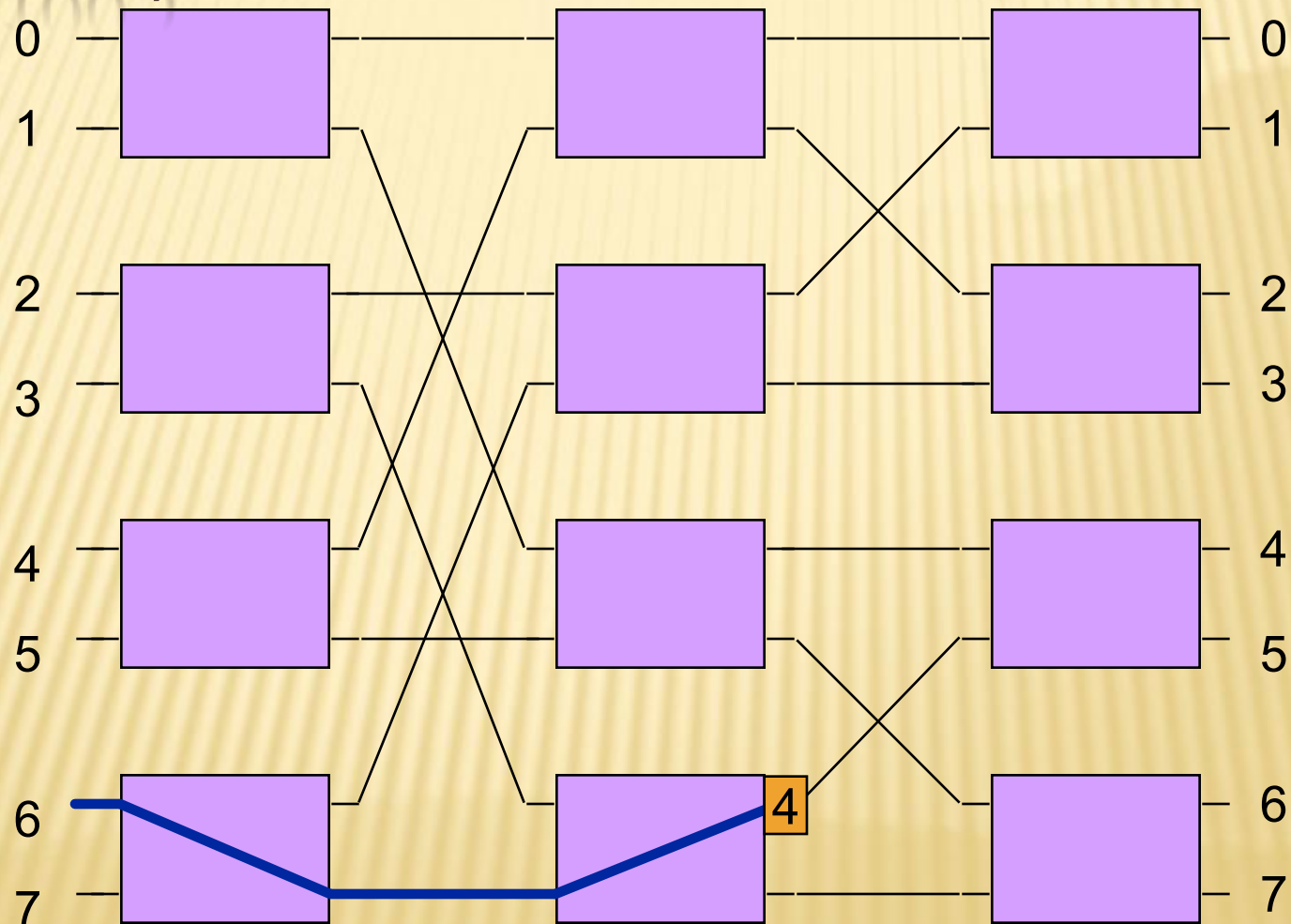
2



EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

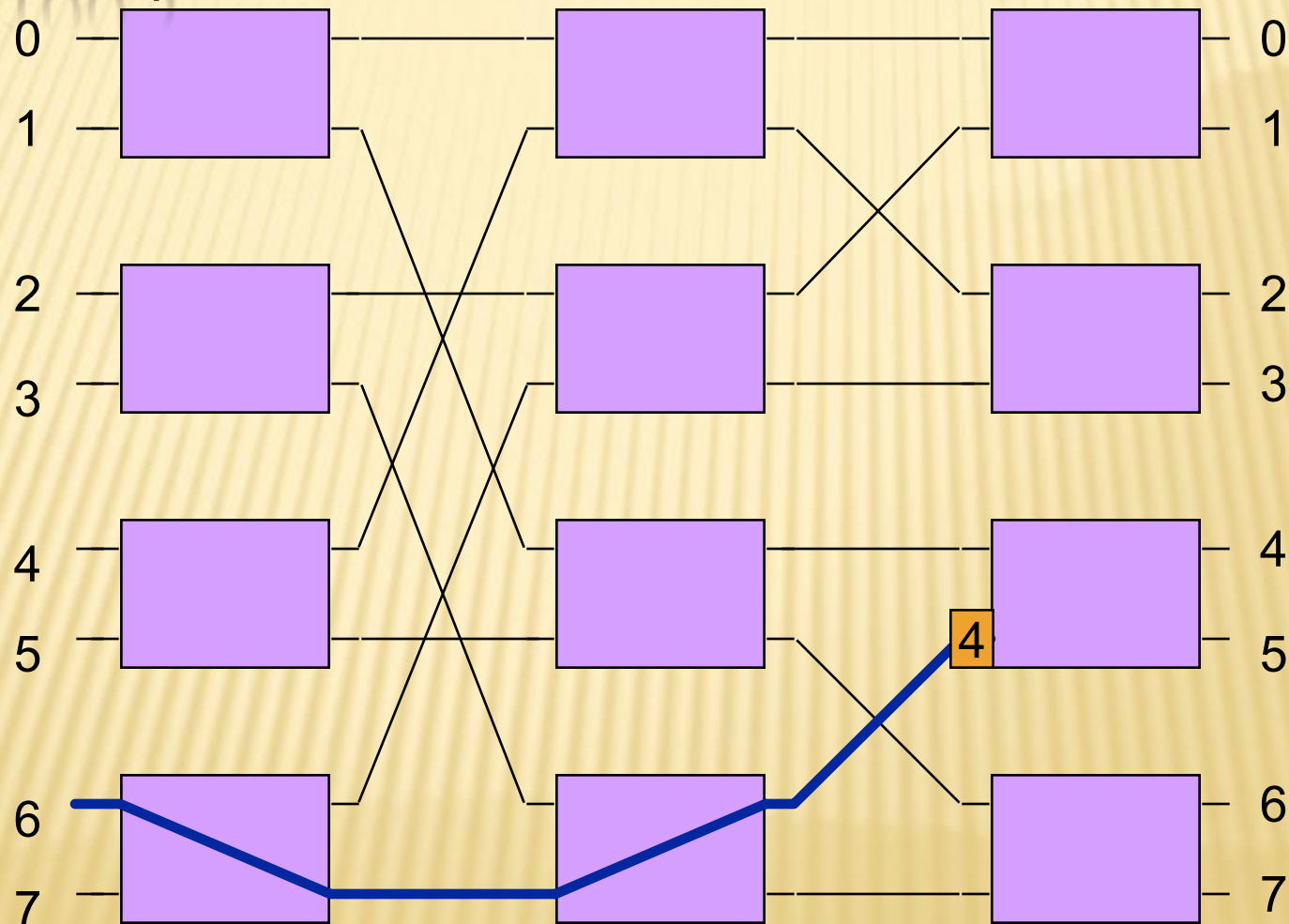
2



EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

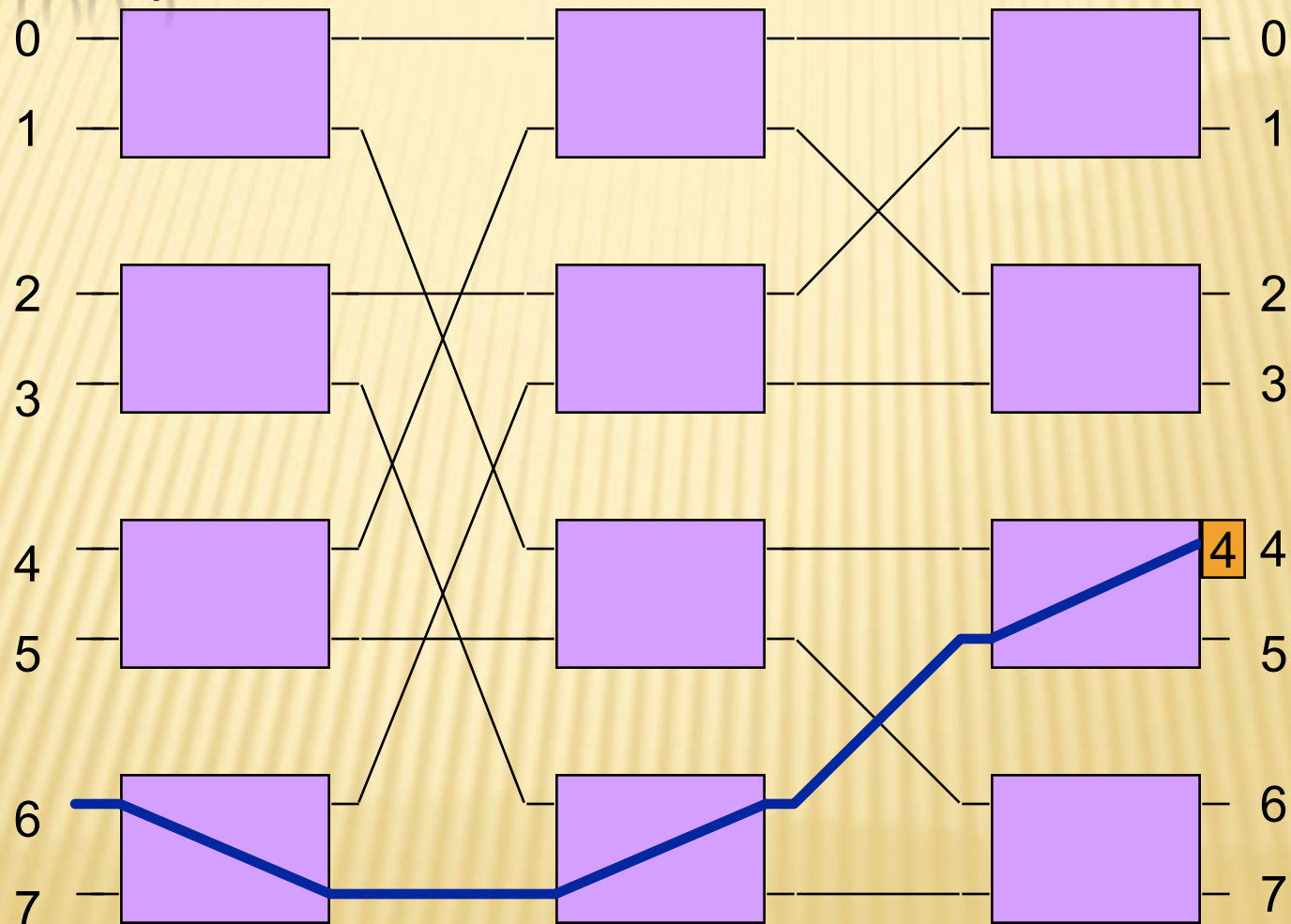
2



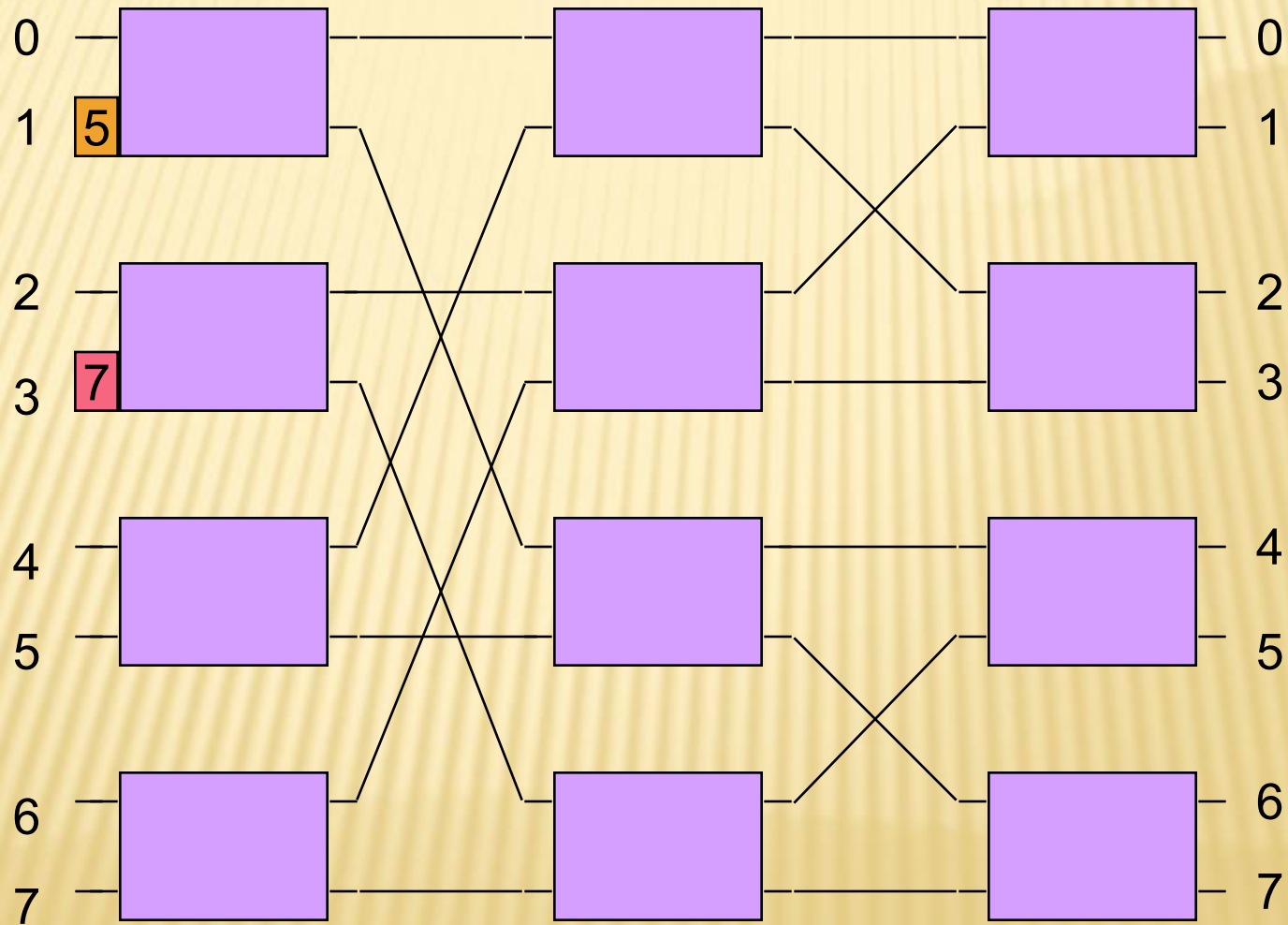
EXAMPLE OF SELF ROUTING

CELL DESTINED FOR OUTPUT PORT 4 (= 100)

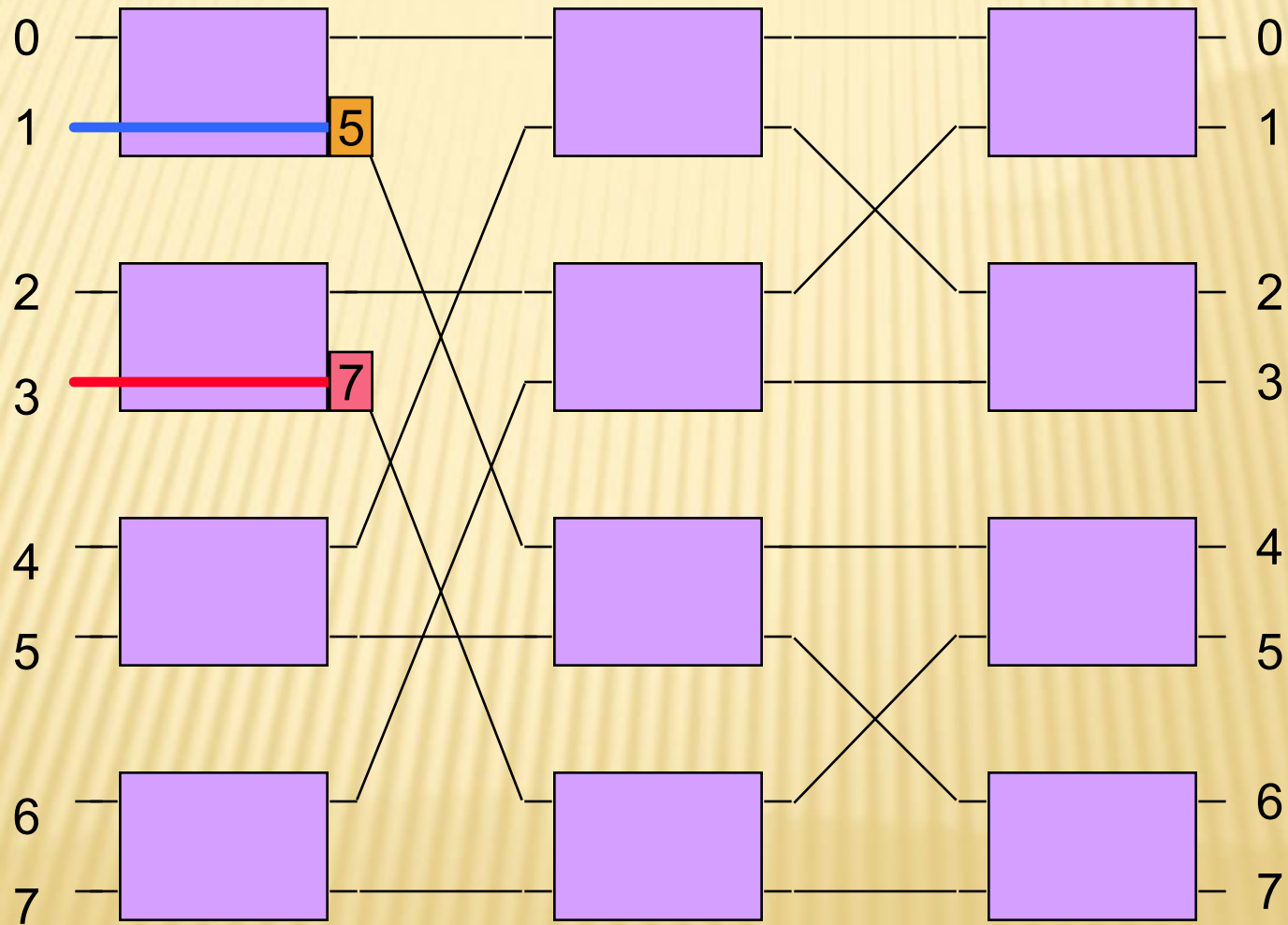
2



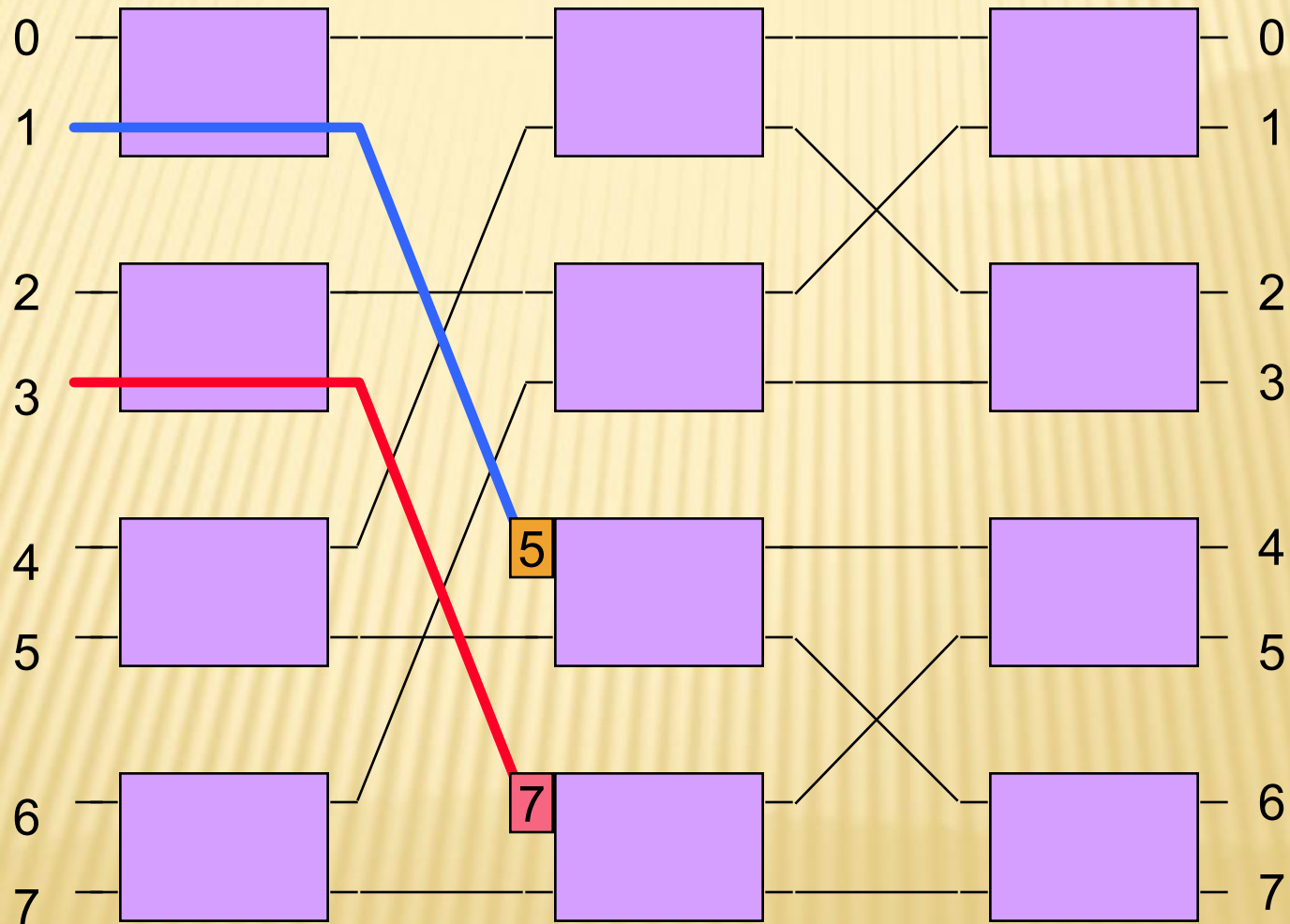
MULTIPLE CONCURRENT PATHS



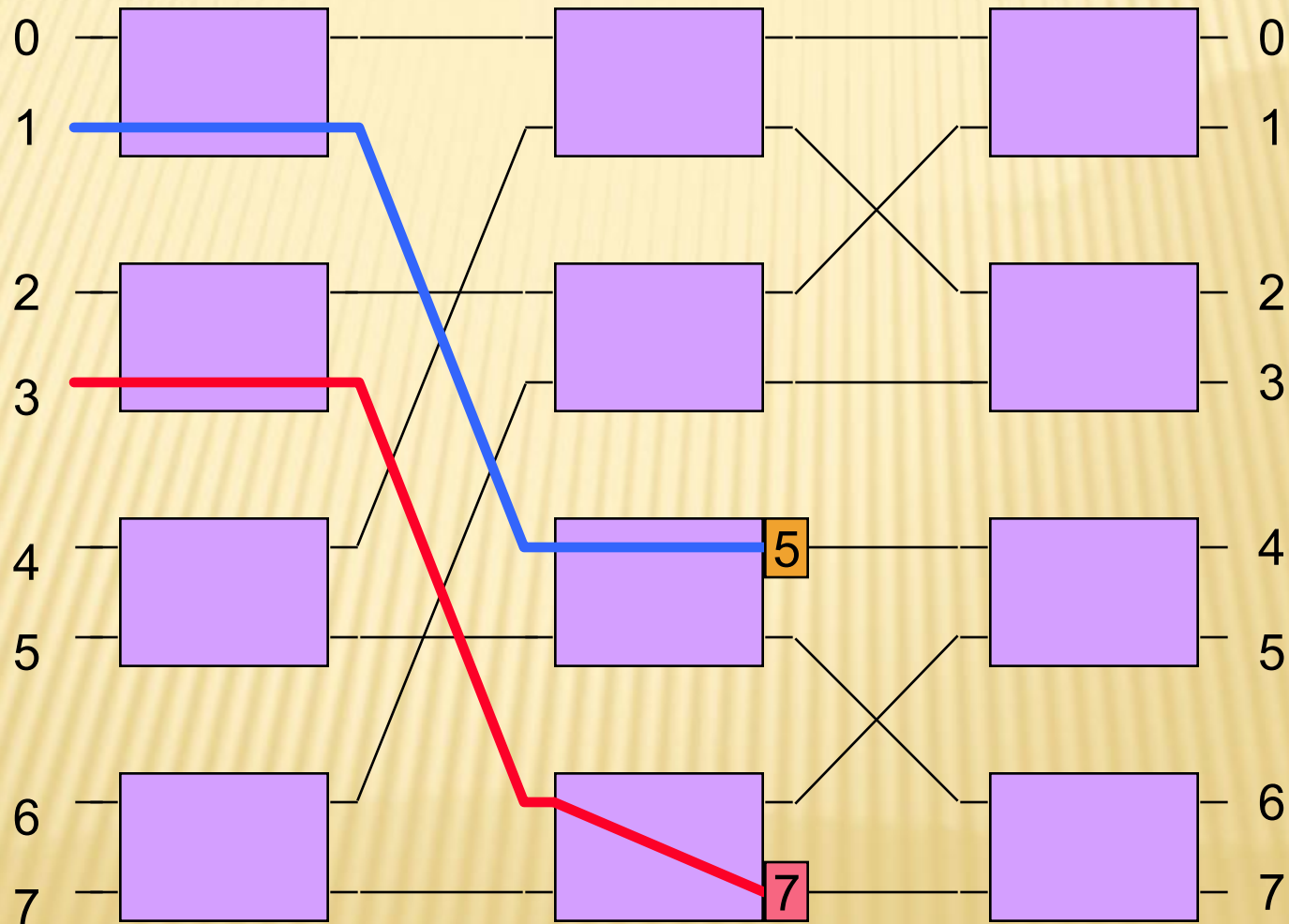
MULTIPLE CONCURRENT PATHS



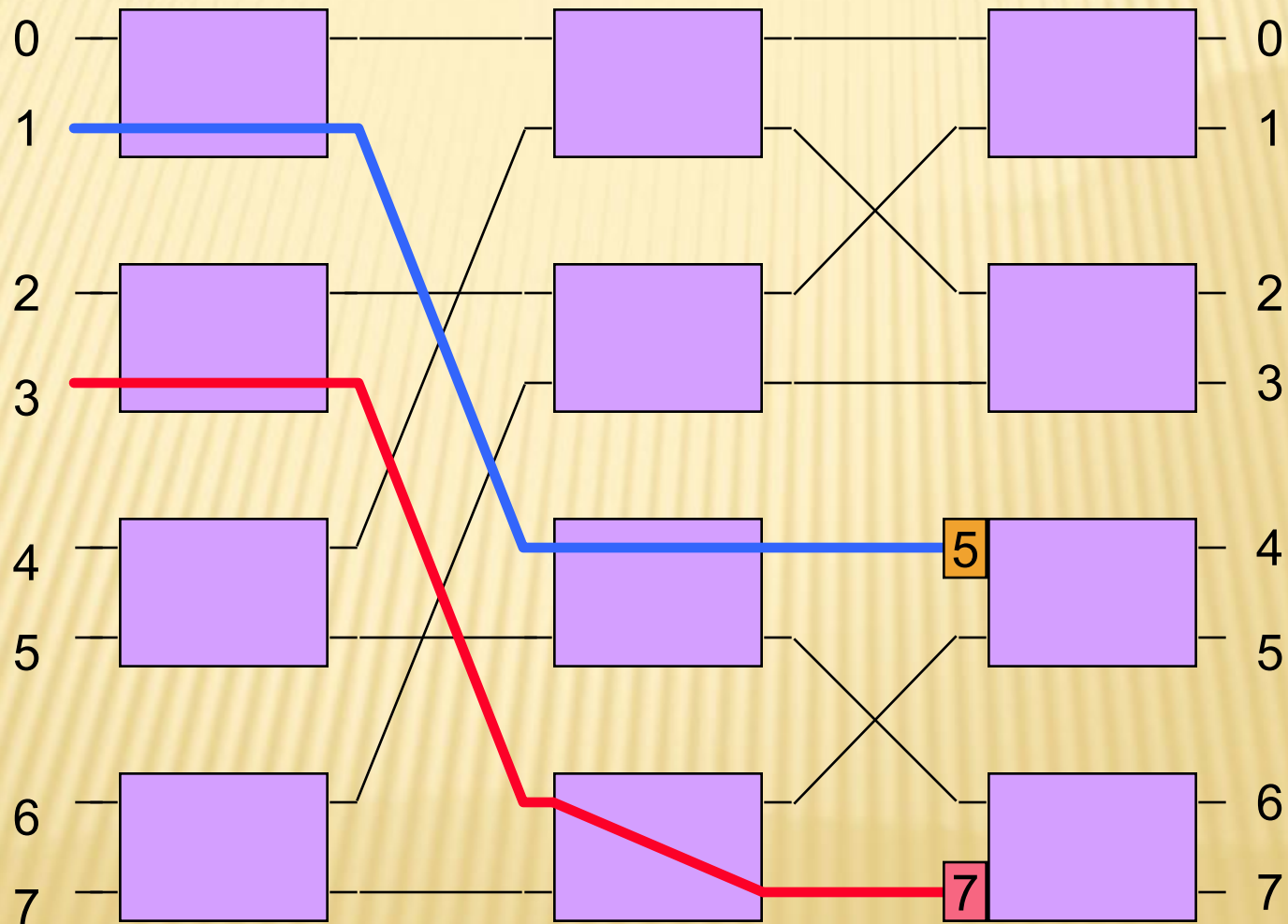
MULTIPLE CONCURRENT PATHS



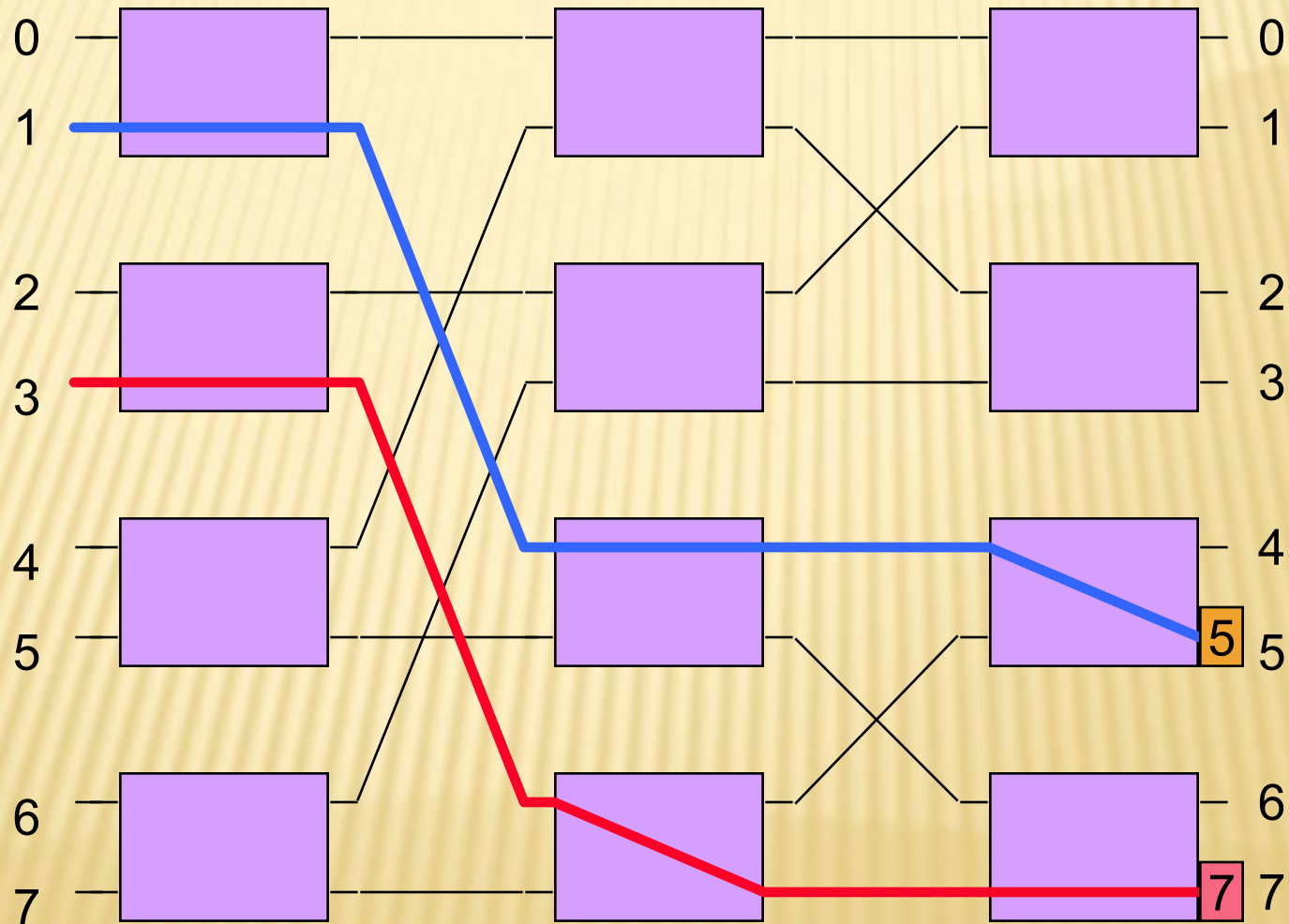
MULTIPLE CONCURRENT PATHS



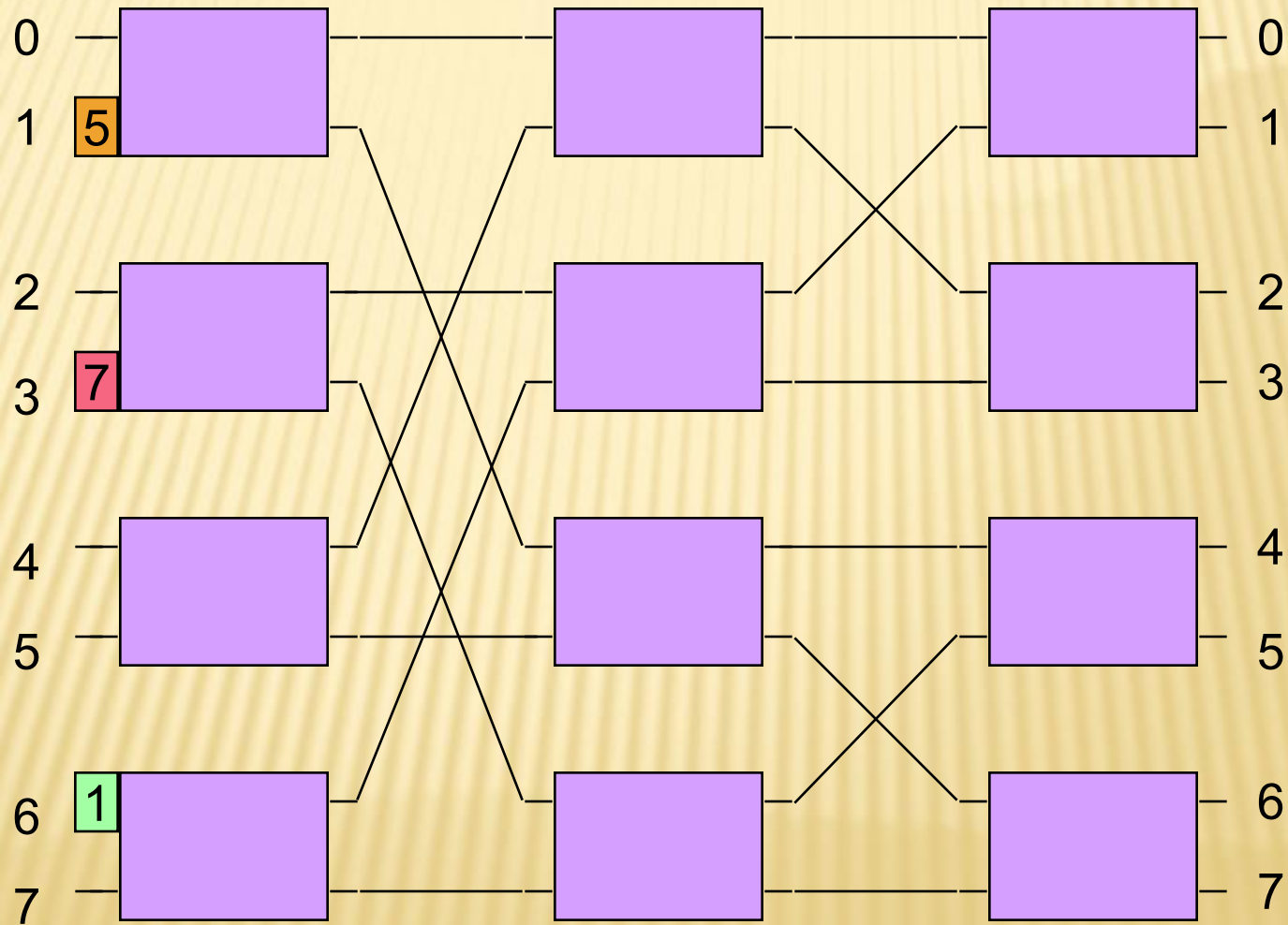
MULTIPLE CONCURRENT PATHS



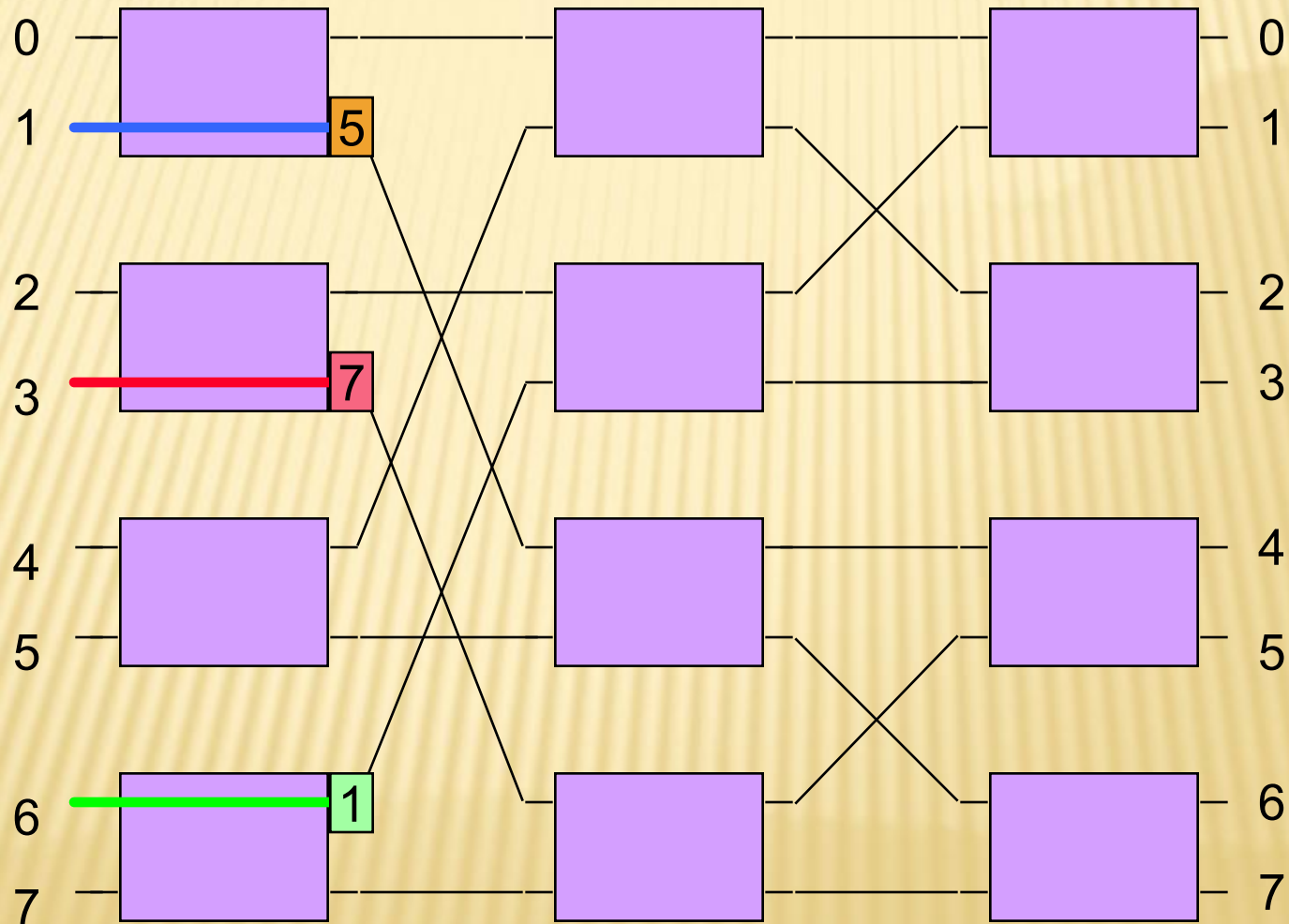
MULTIPLE CONCURRENT PATHS



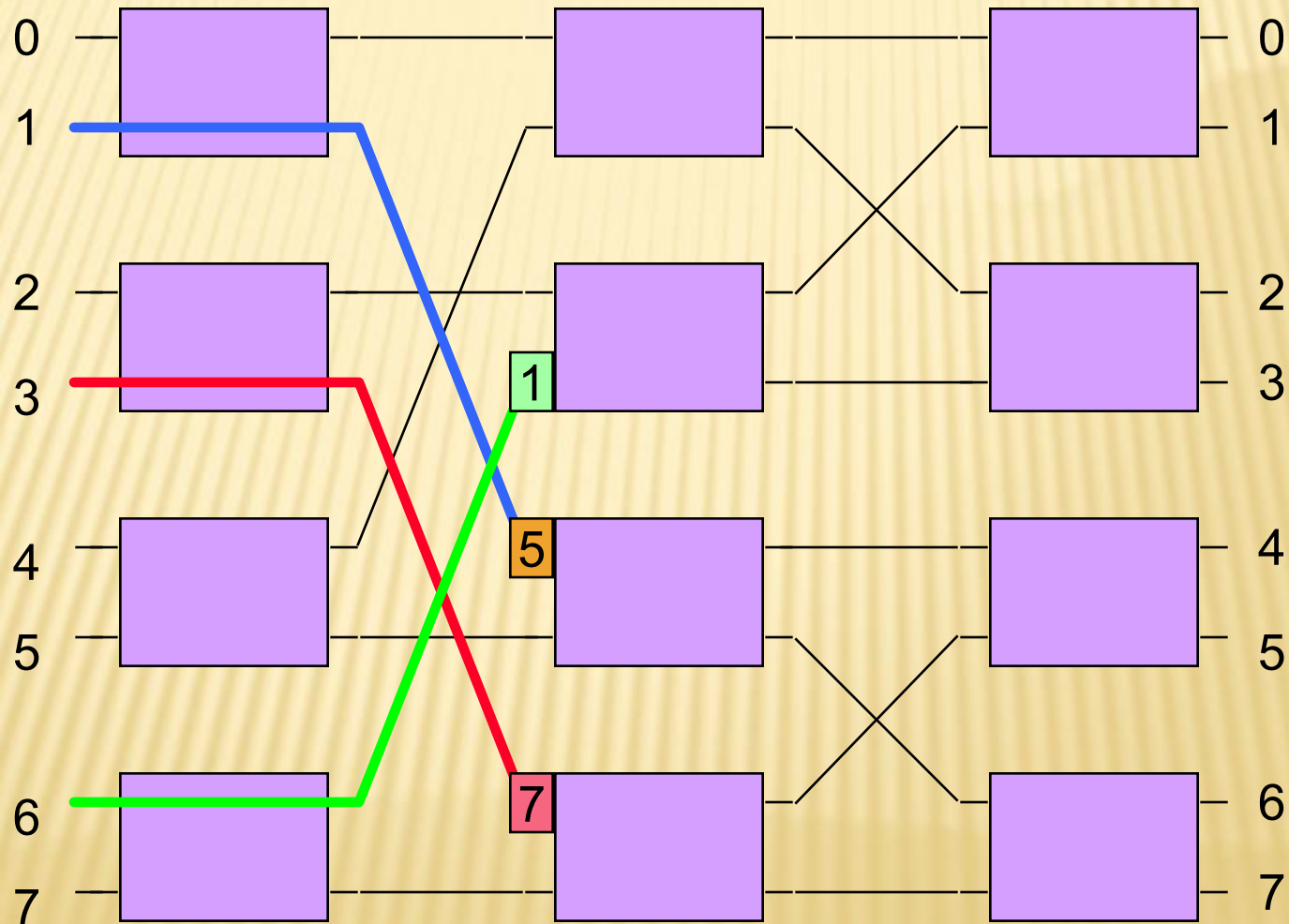
MULTIPLE CONCURRENT PATHS



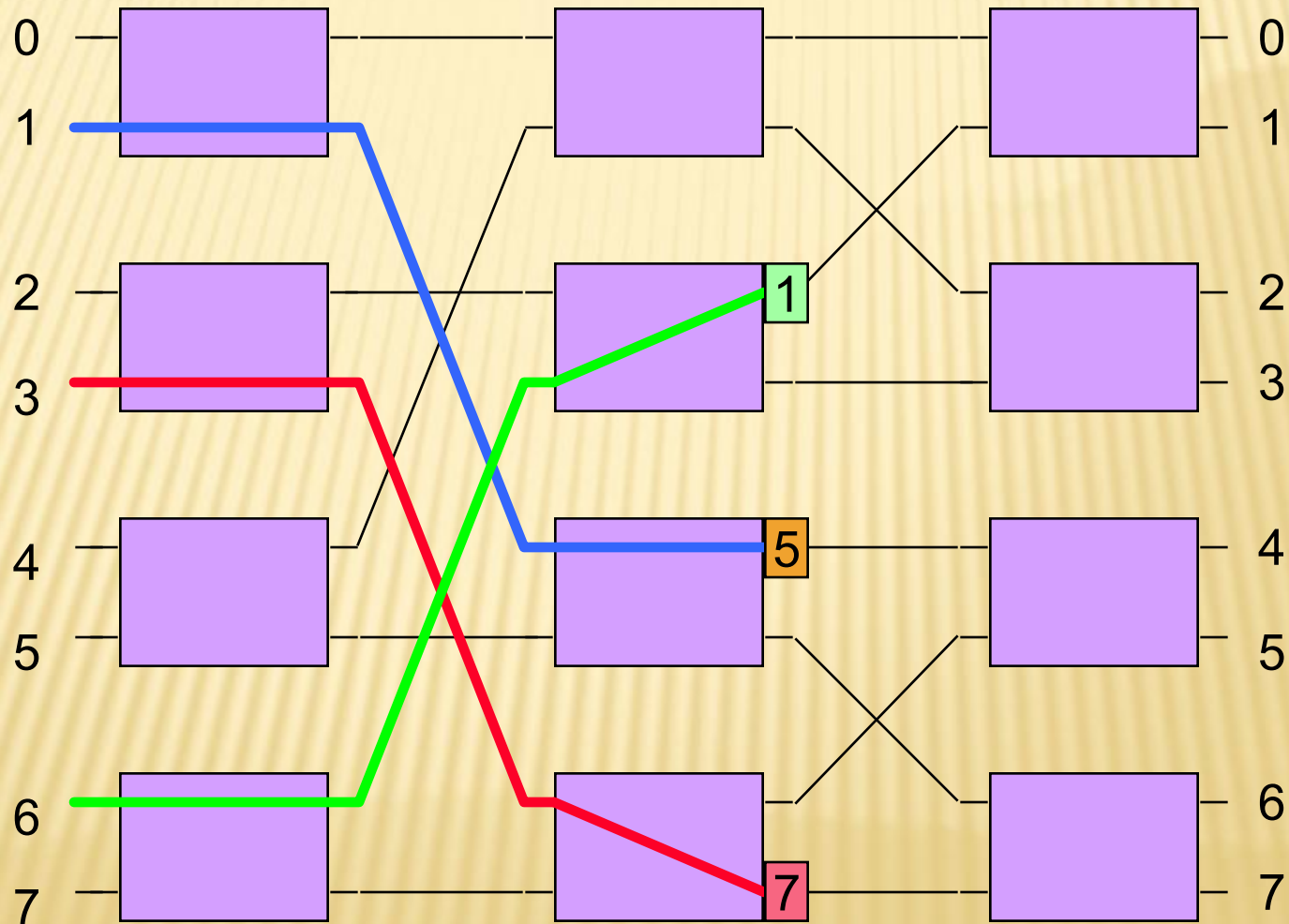
MULTIPLE CONCURRENT PATHS



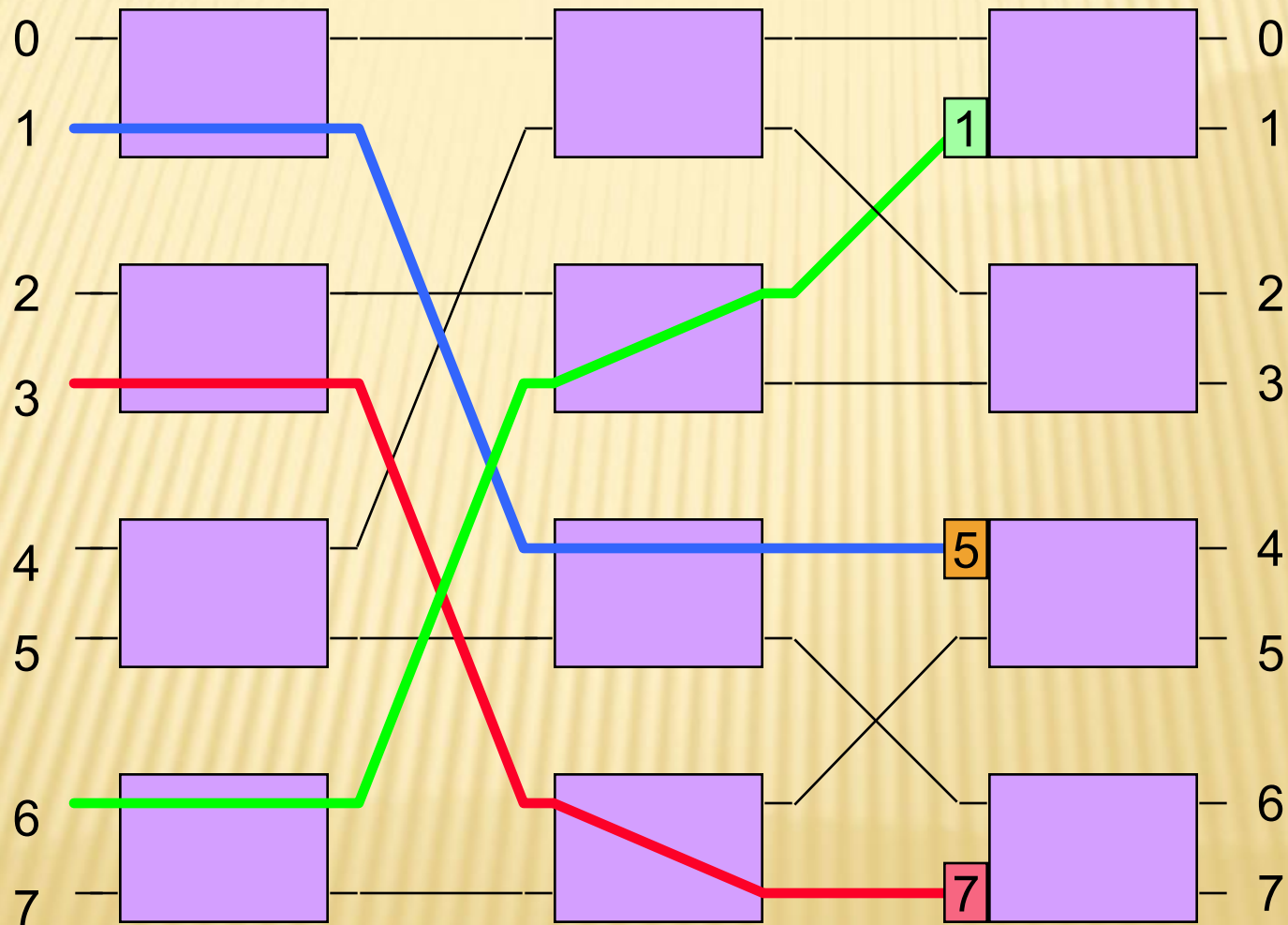
MULTIPLE CONCURRENT PATHS



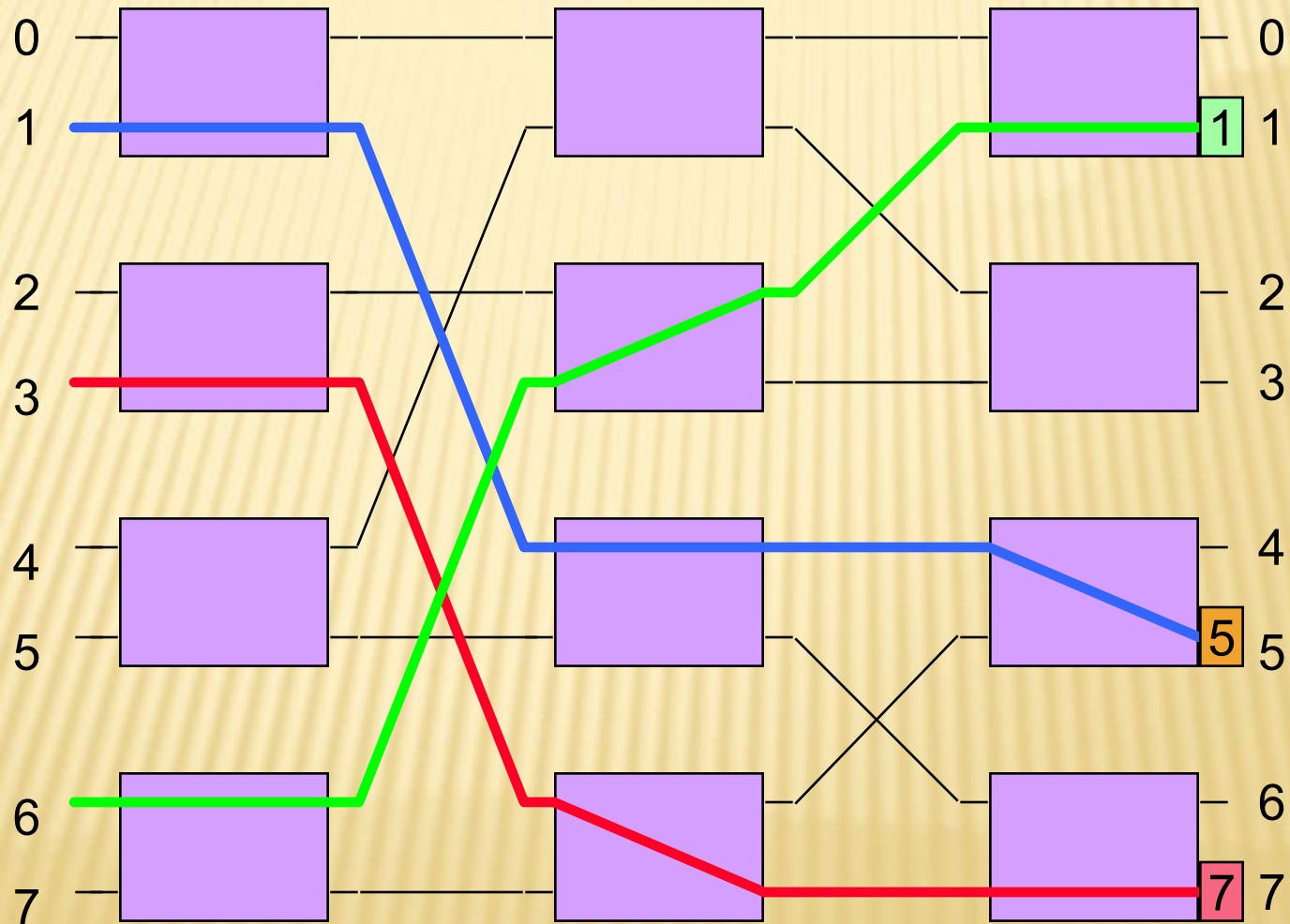
MULTIPLE CONCURRENT PATHS



MULTIPLE CONCURRENT PATHS



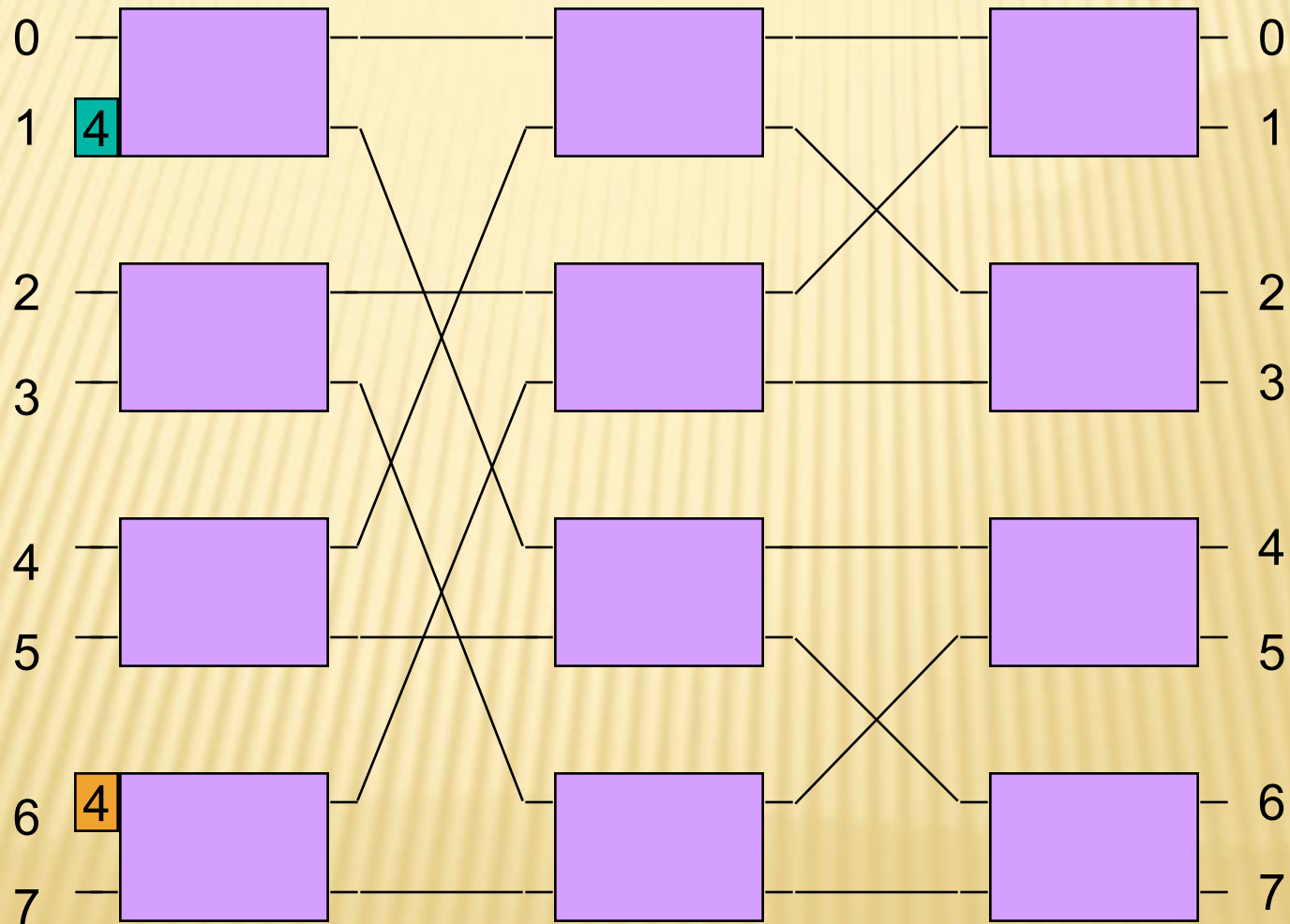
MULTIPLE CONCURRENT PATHS



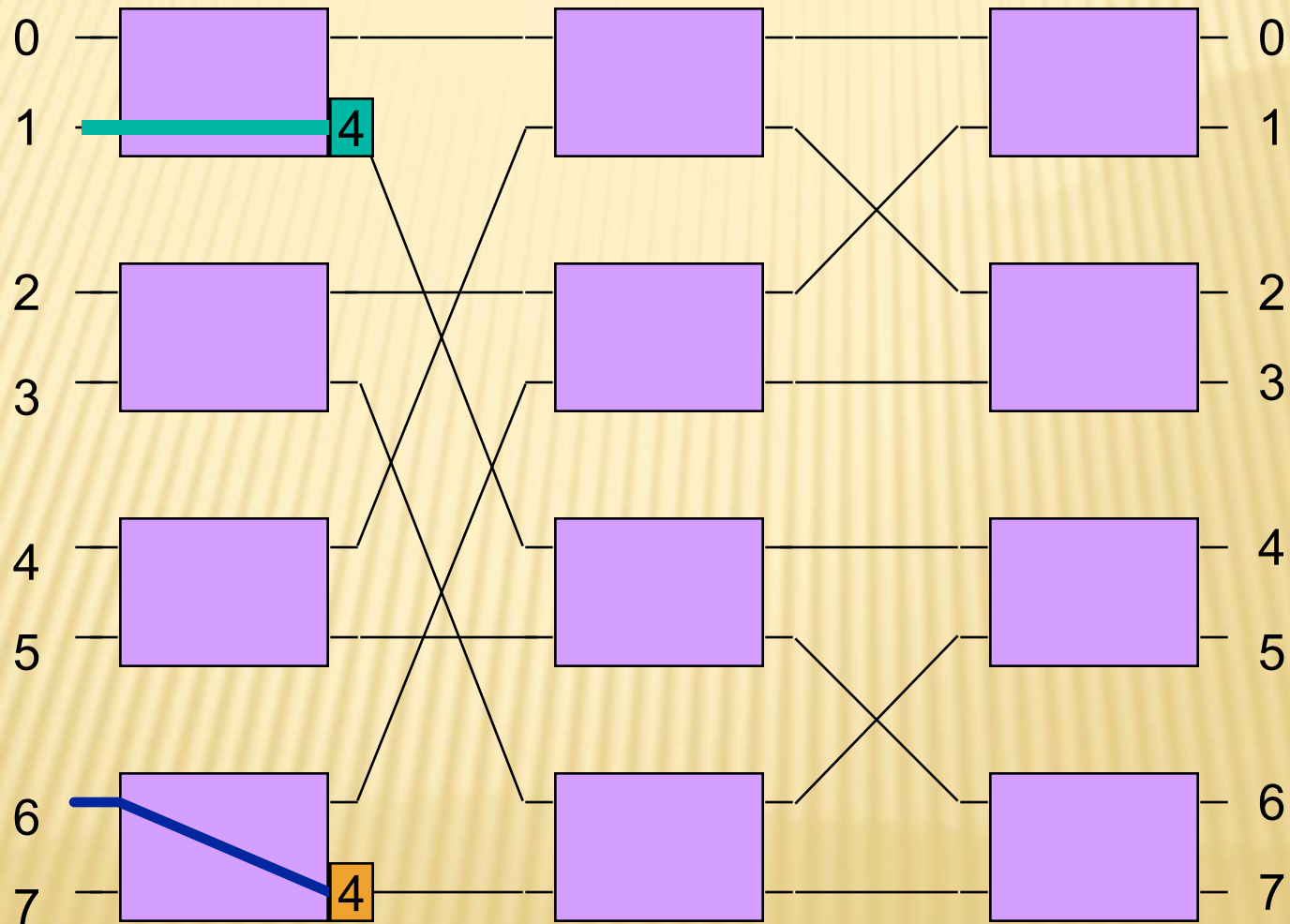
OUTPUT PORT CONTENTION

- Up to now, all examples have worked wonderfully because each incoming cell was destined to a different output port
- What happens if more than one cell destined to same output port?
- Answer: output port contention
- Result: cell loss in a bufferless network

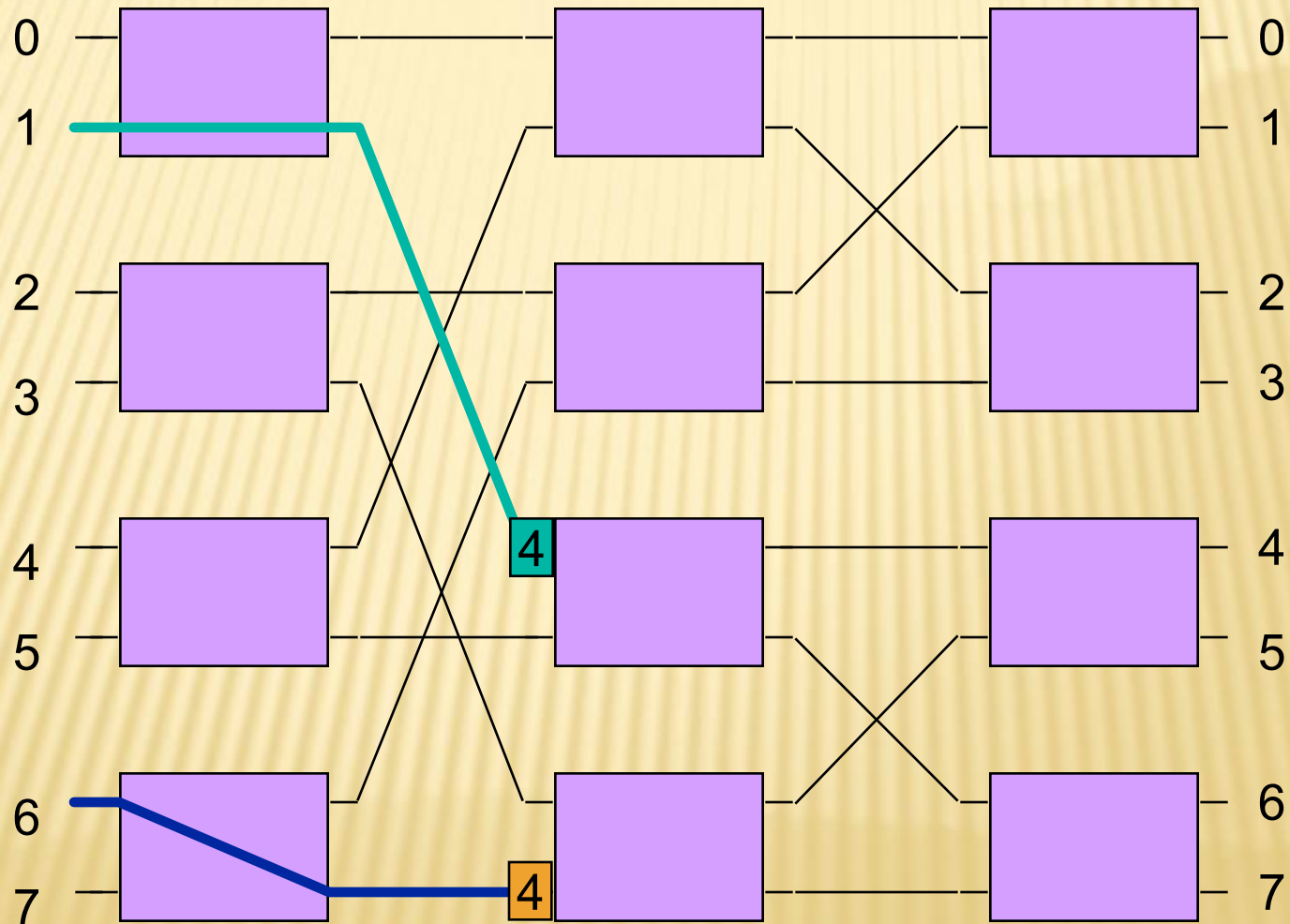
OUTPUT PORT CONTENTION



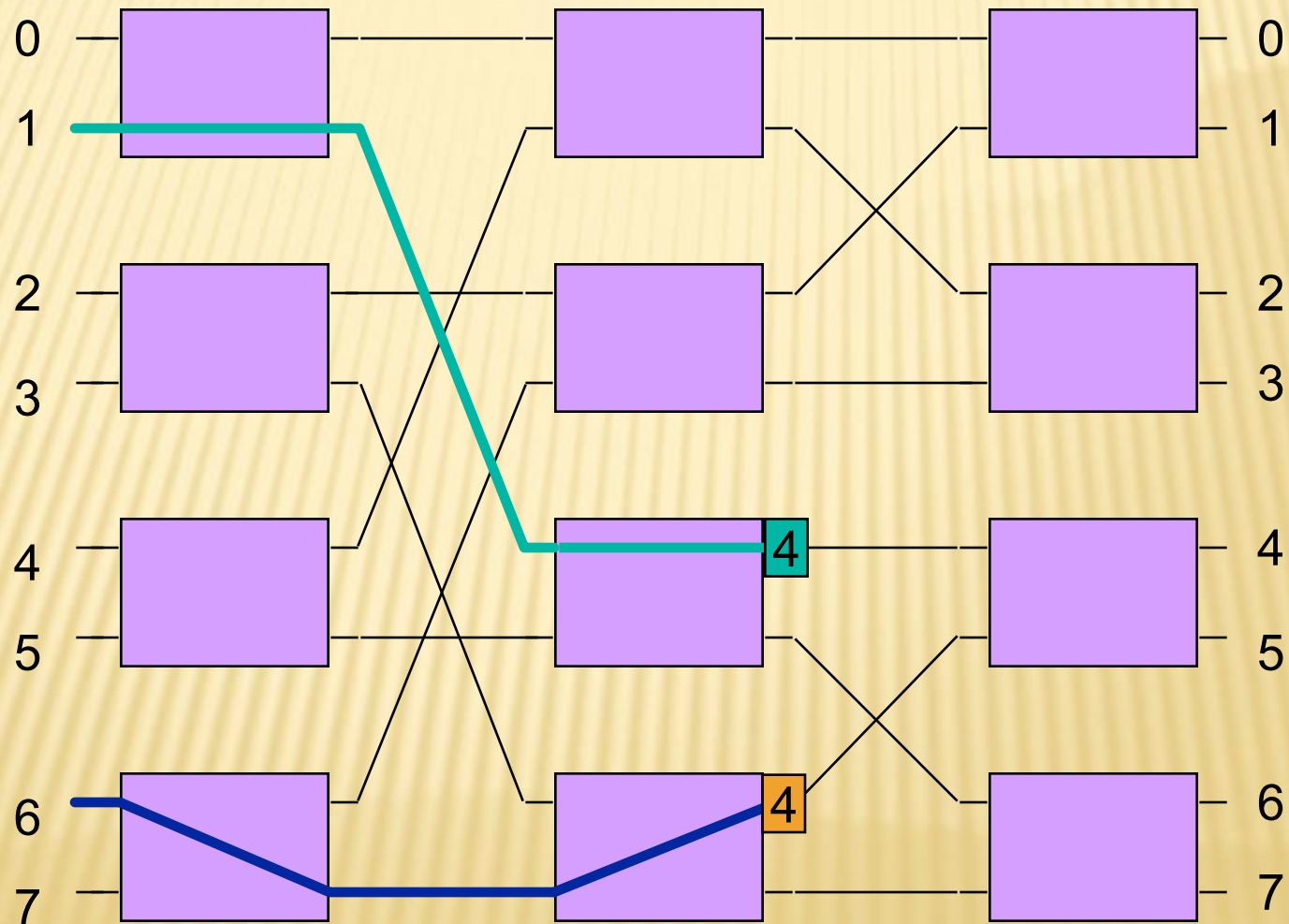
OUTPUT PORT CONTENTION



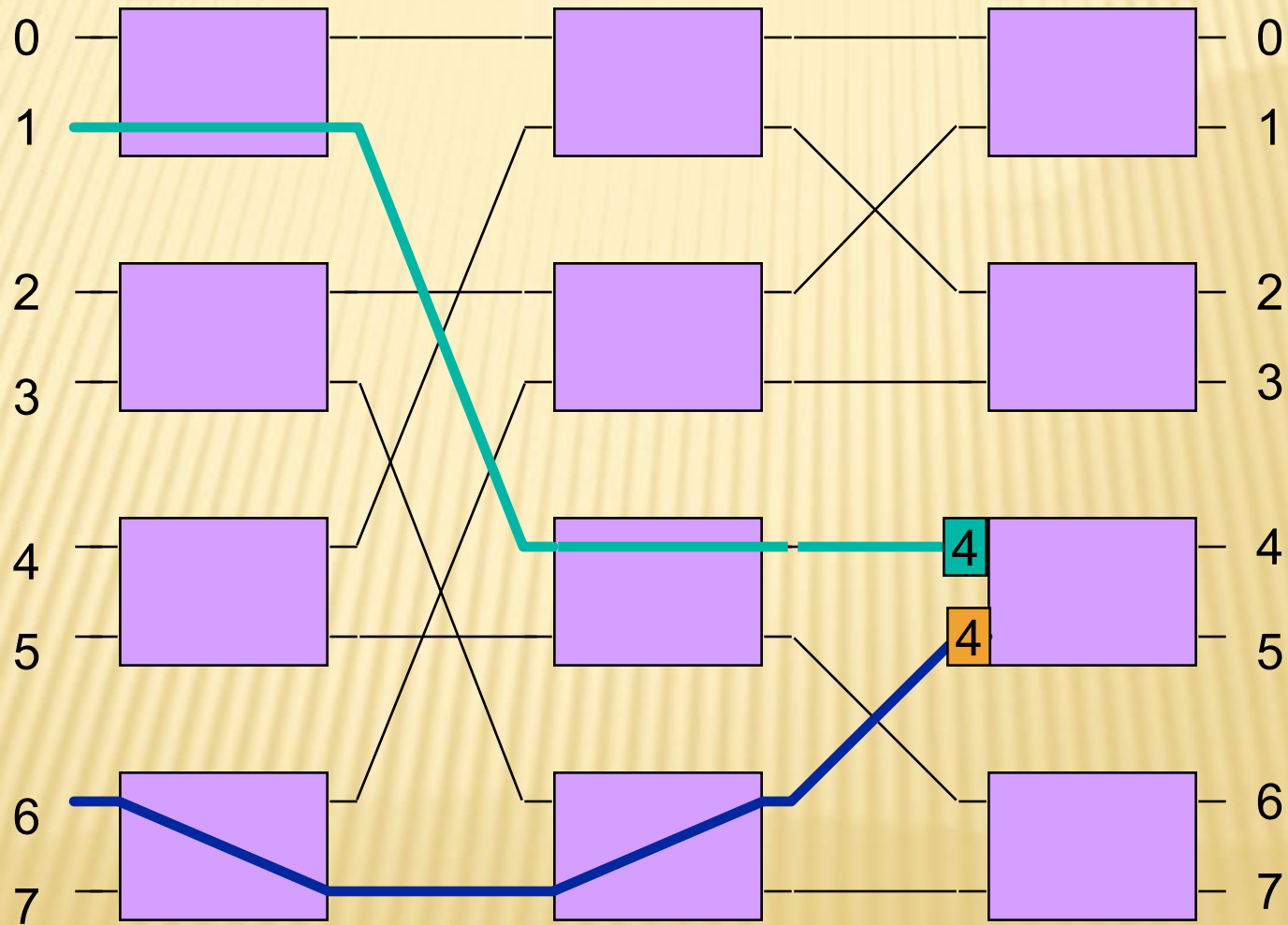
OUTPUT PORT CONTENTION



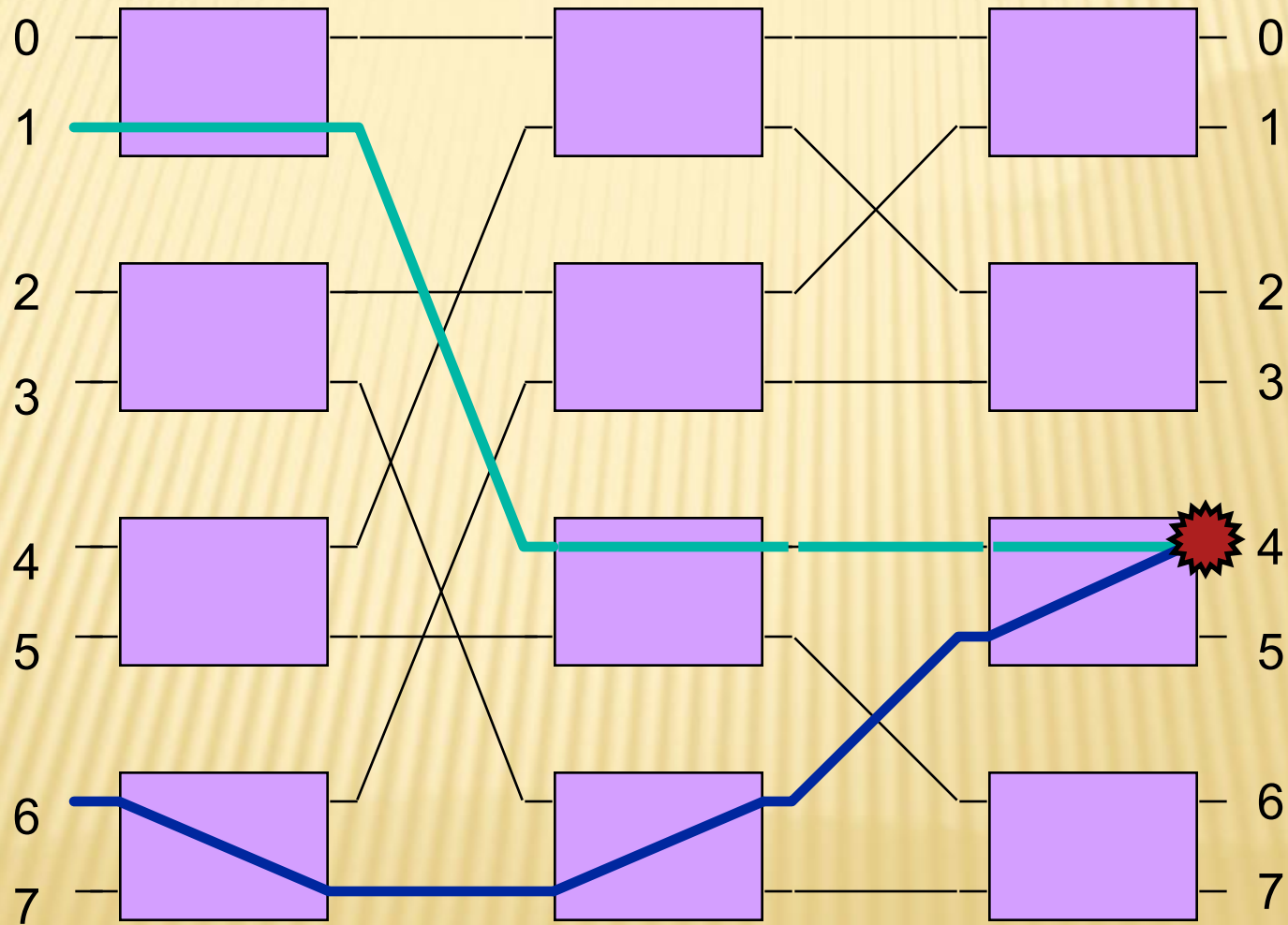
OUTPUT PORT CONTENTION



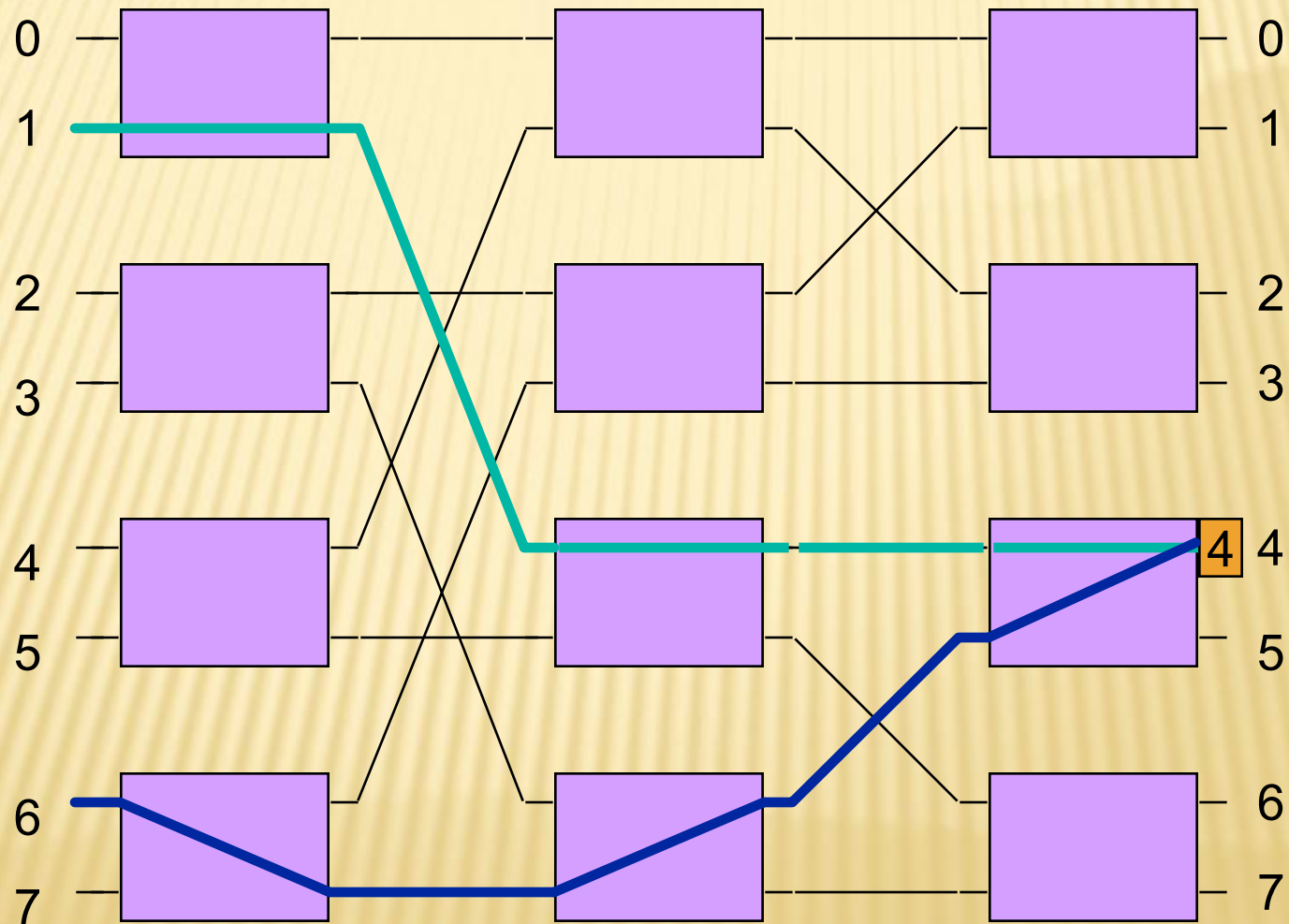
OUTPUT PORT CONTENTION



OUTPUT PORT CONTENTION



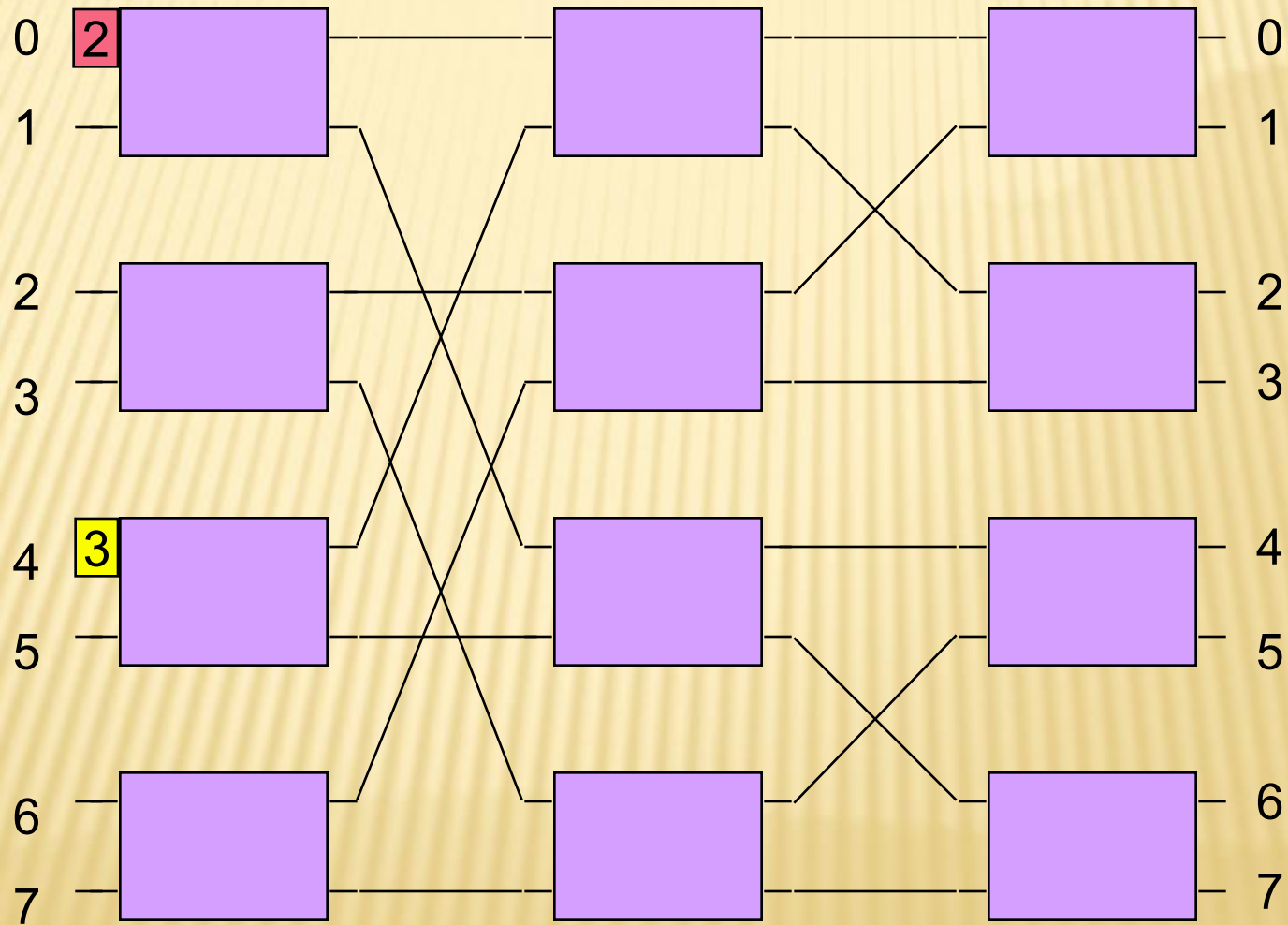
OUTPUT PORT CONTENTION



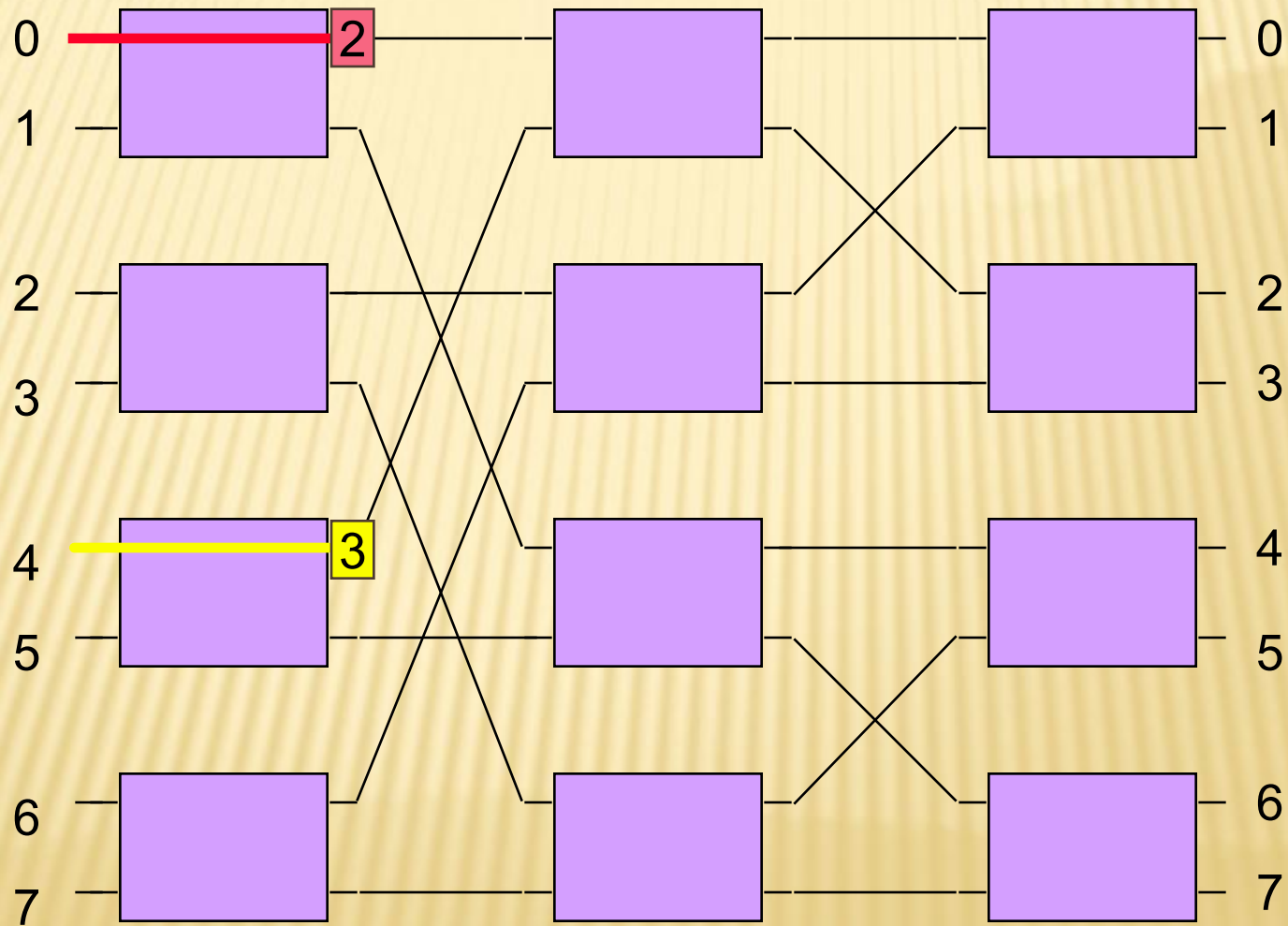
PATH CONTENTION

- ✖ It is also possible for two incoming cells that are destined to different output ports to require the same internal link in the switch
- ✖ Called path contention or internal blocking
- ✖ Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- ✖ Path contention and output port contention can seriously degrade the achievable throughput of the switch

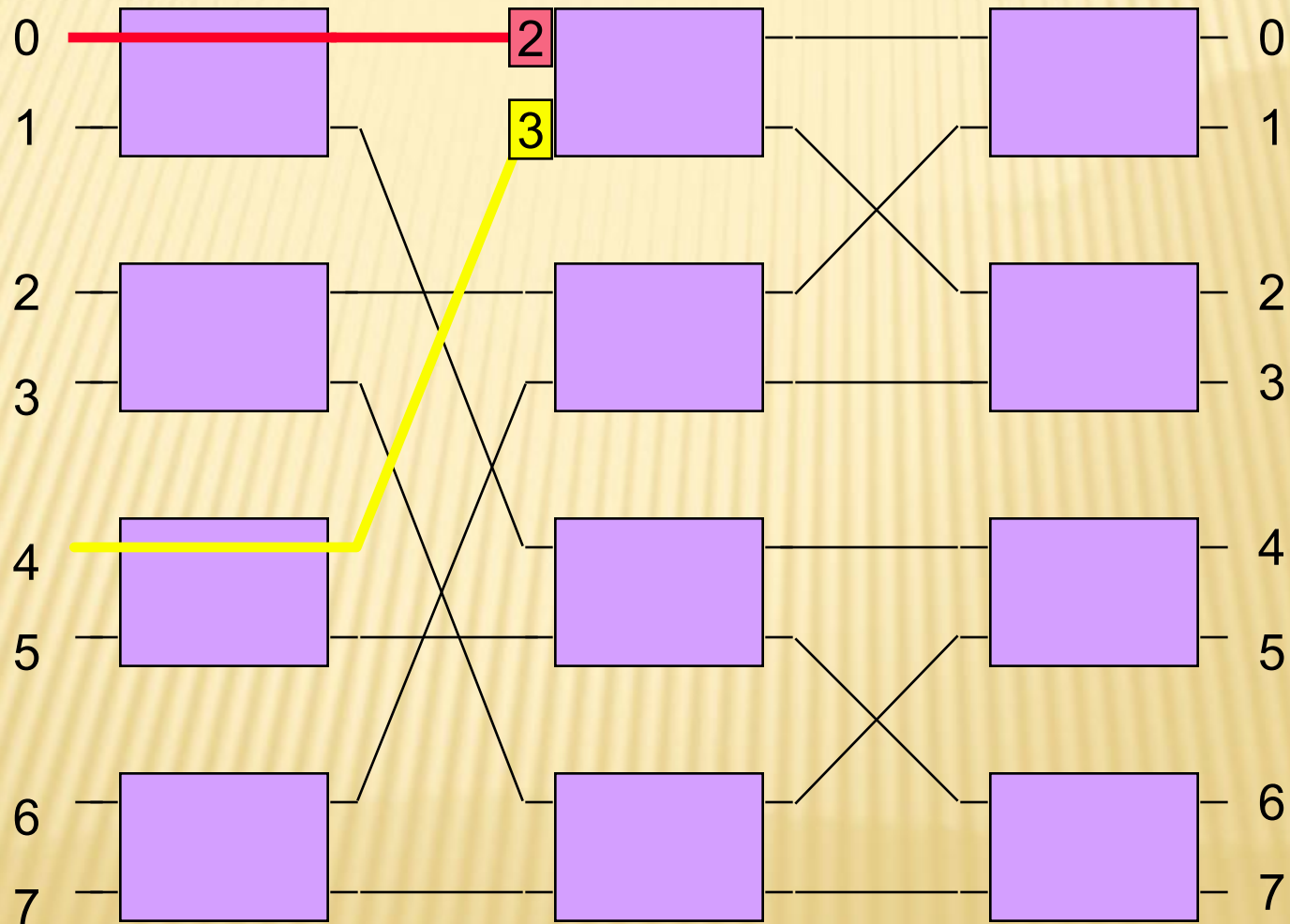
PATH CONTENTION



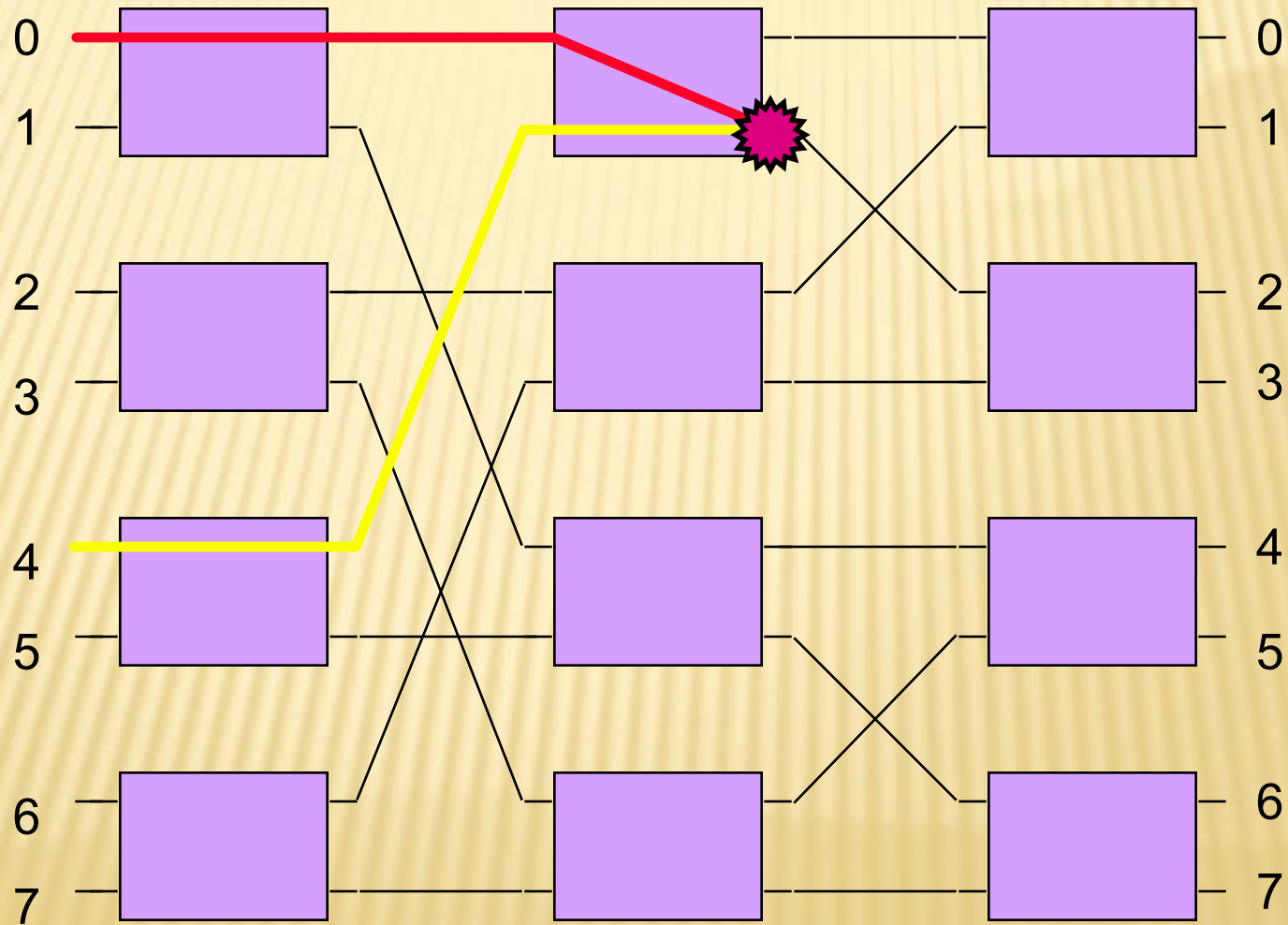
PATH CONTENTION



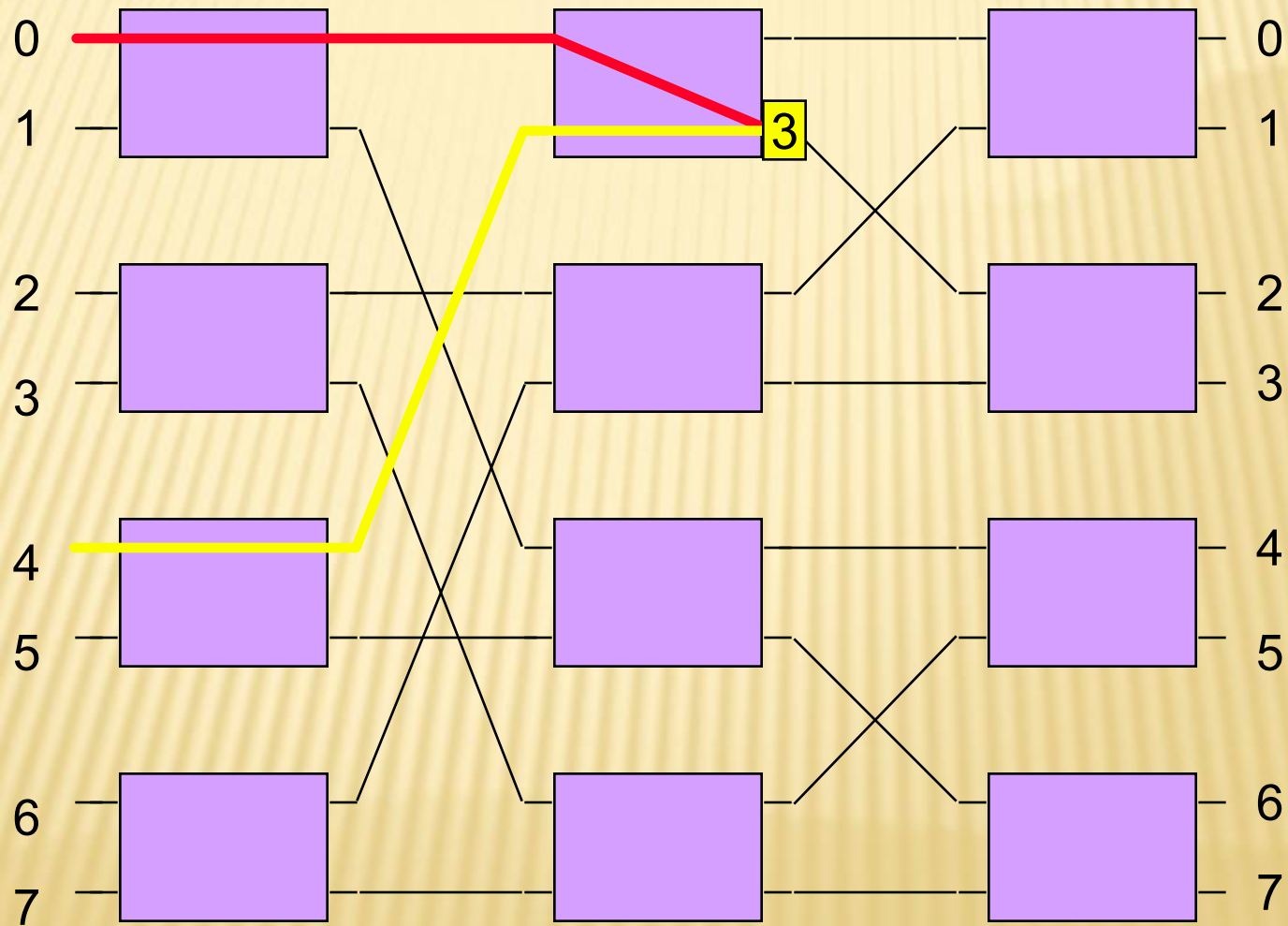
PATH CONTENTION



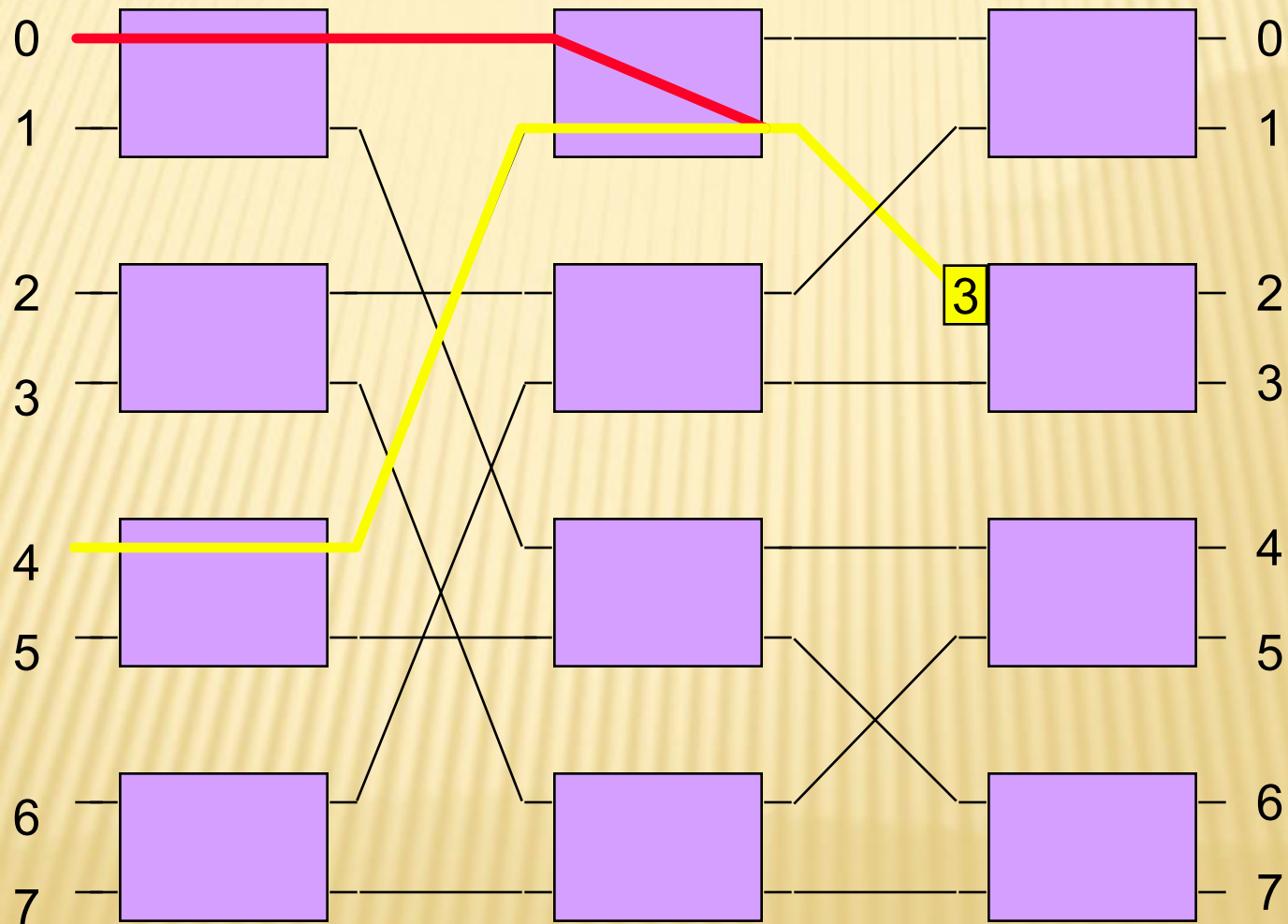
PATH CONTENTION



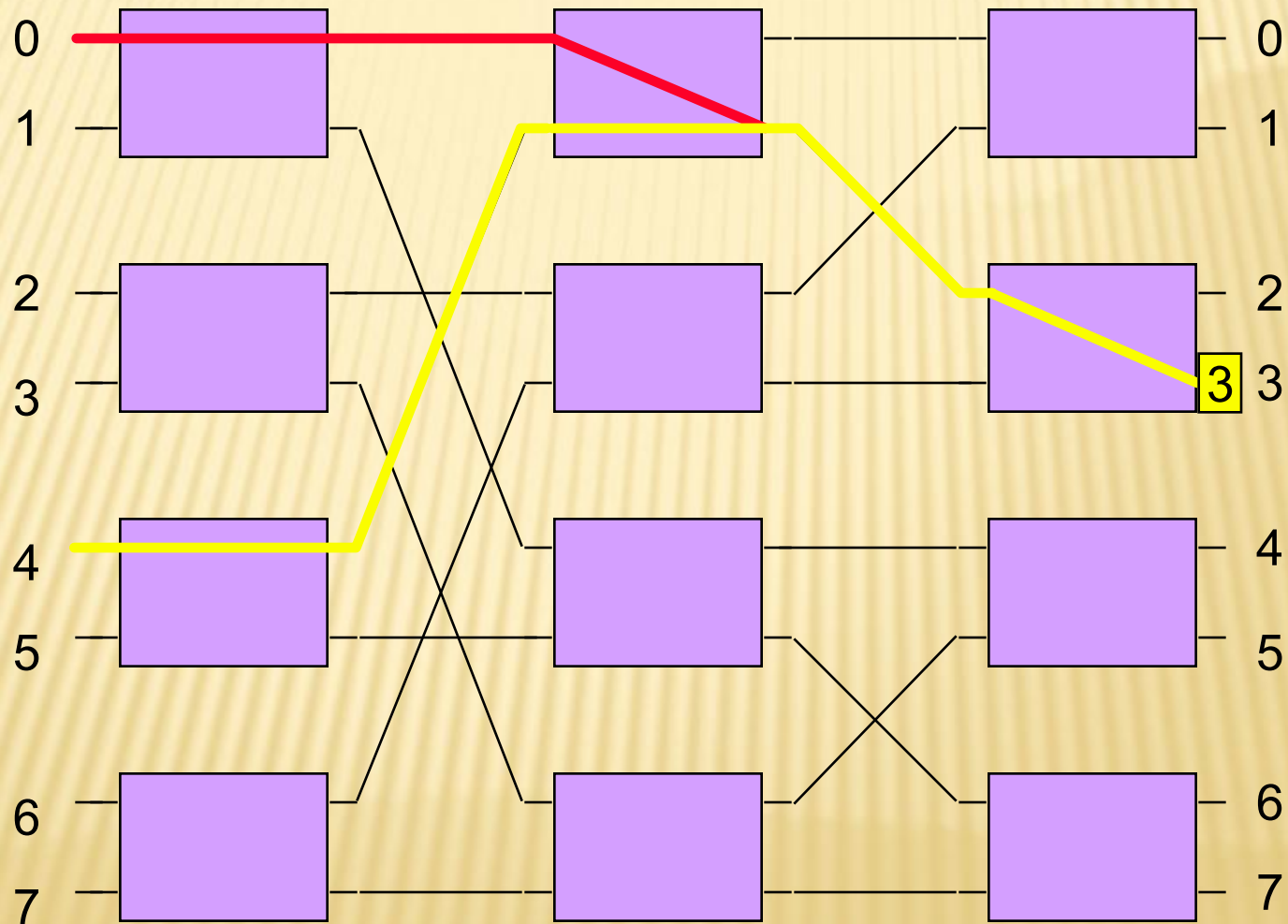
PATH CONTENTION



PATH CONTENTION

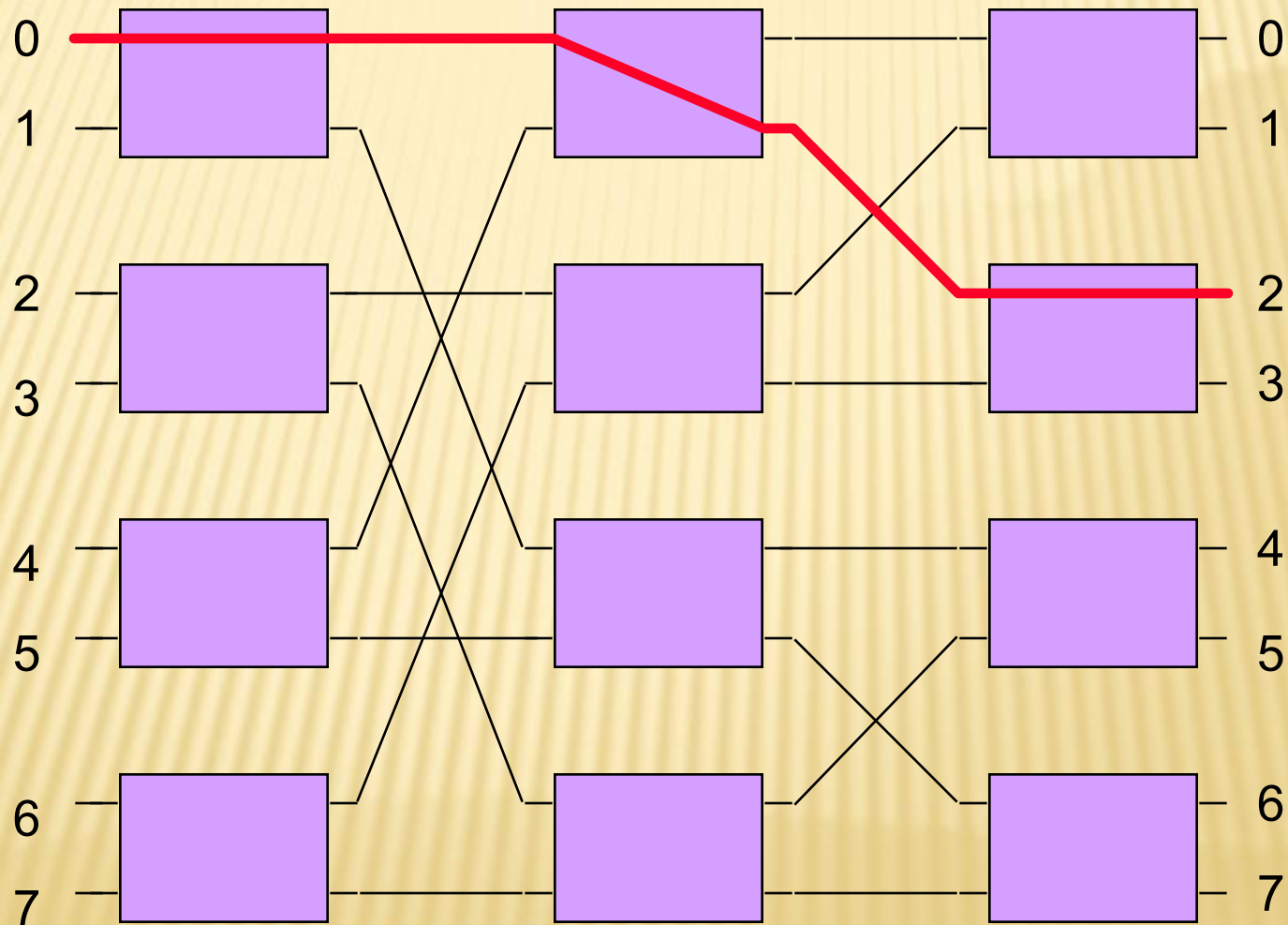


PATH CONTENTION



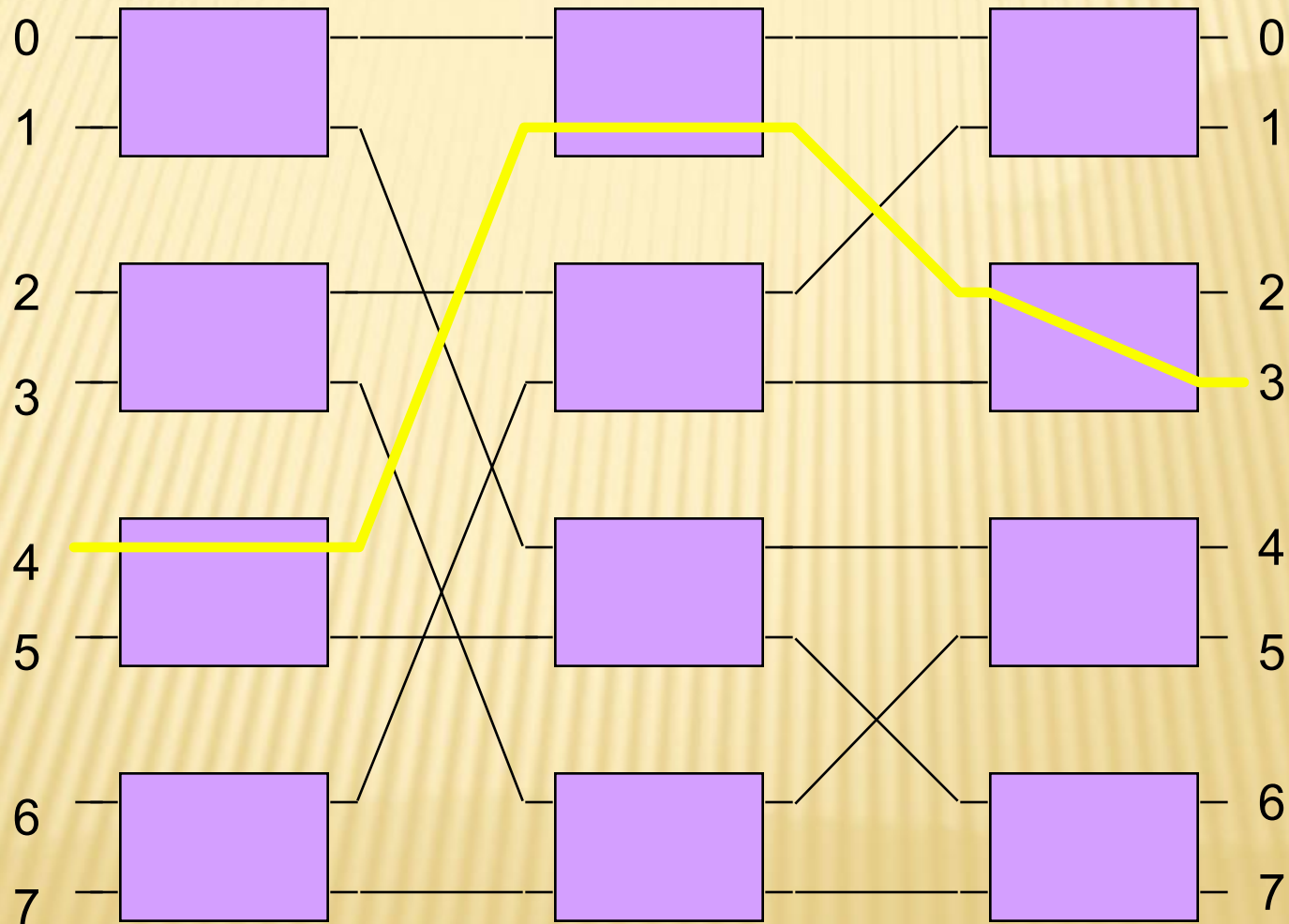
8 X 8 DELTA NETWORK

Cell on input port 0 destined for output port 2



8 x 8 DELTA NETWORK

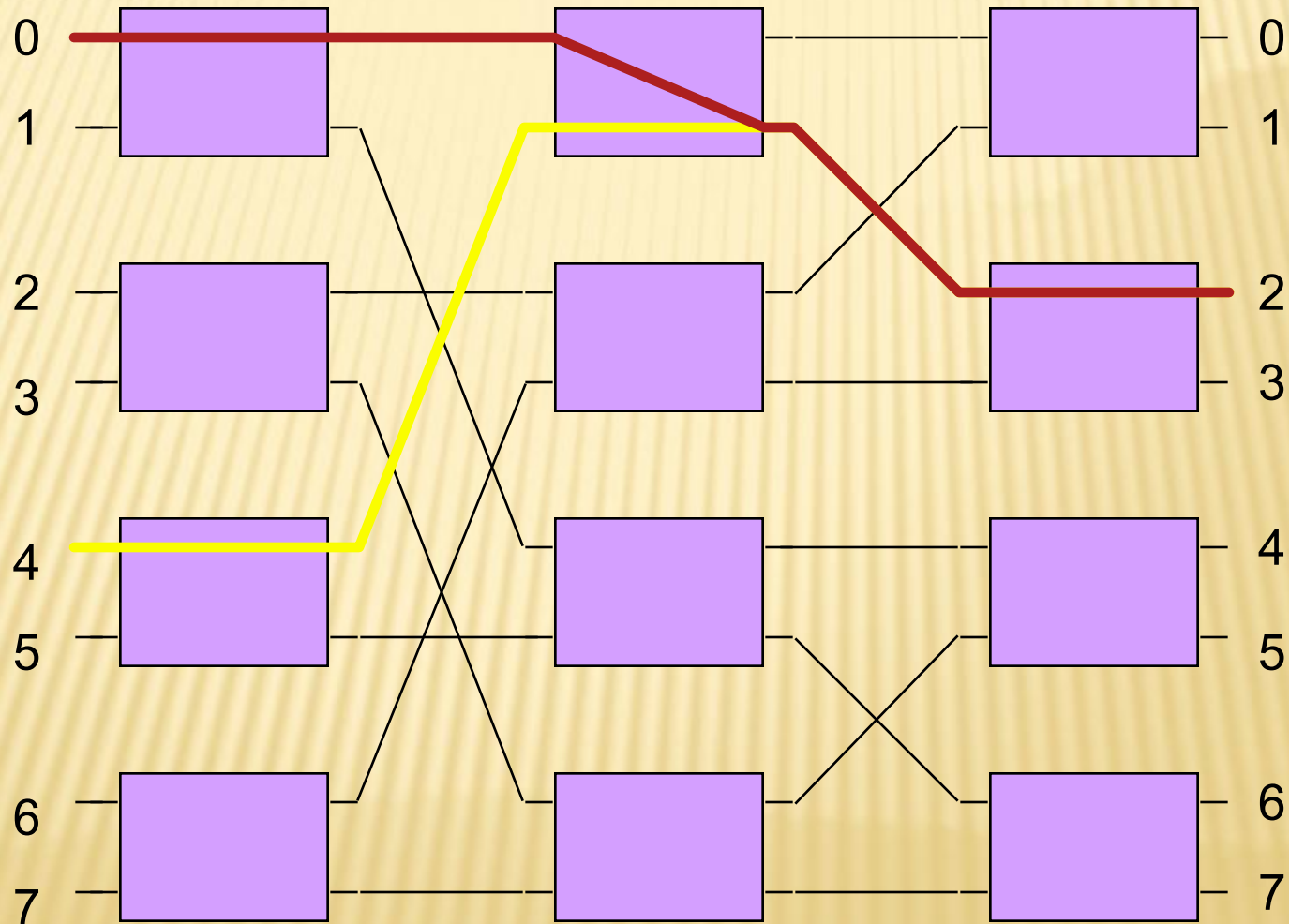
Cell on input port 4 destined for output port 3



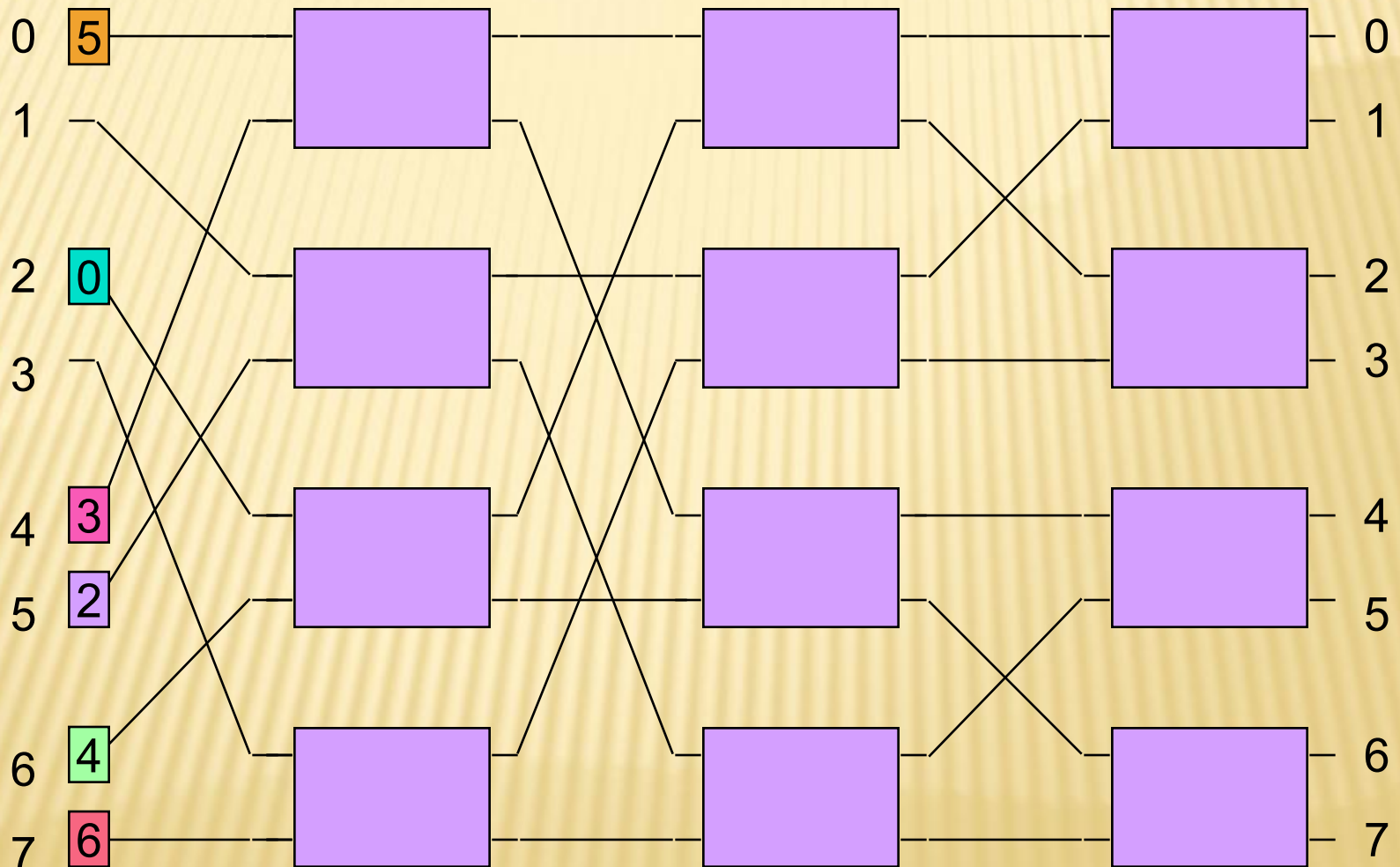
INTERNAL BLOCKING

Cell on input port 0 destined for output port 2

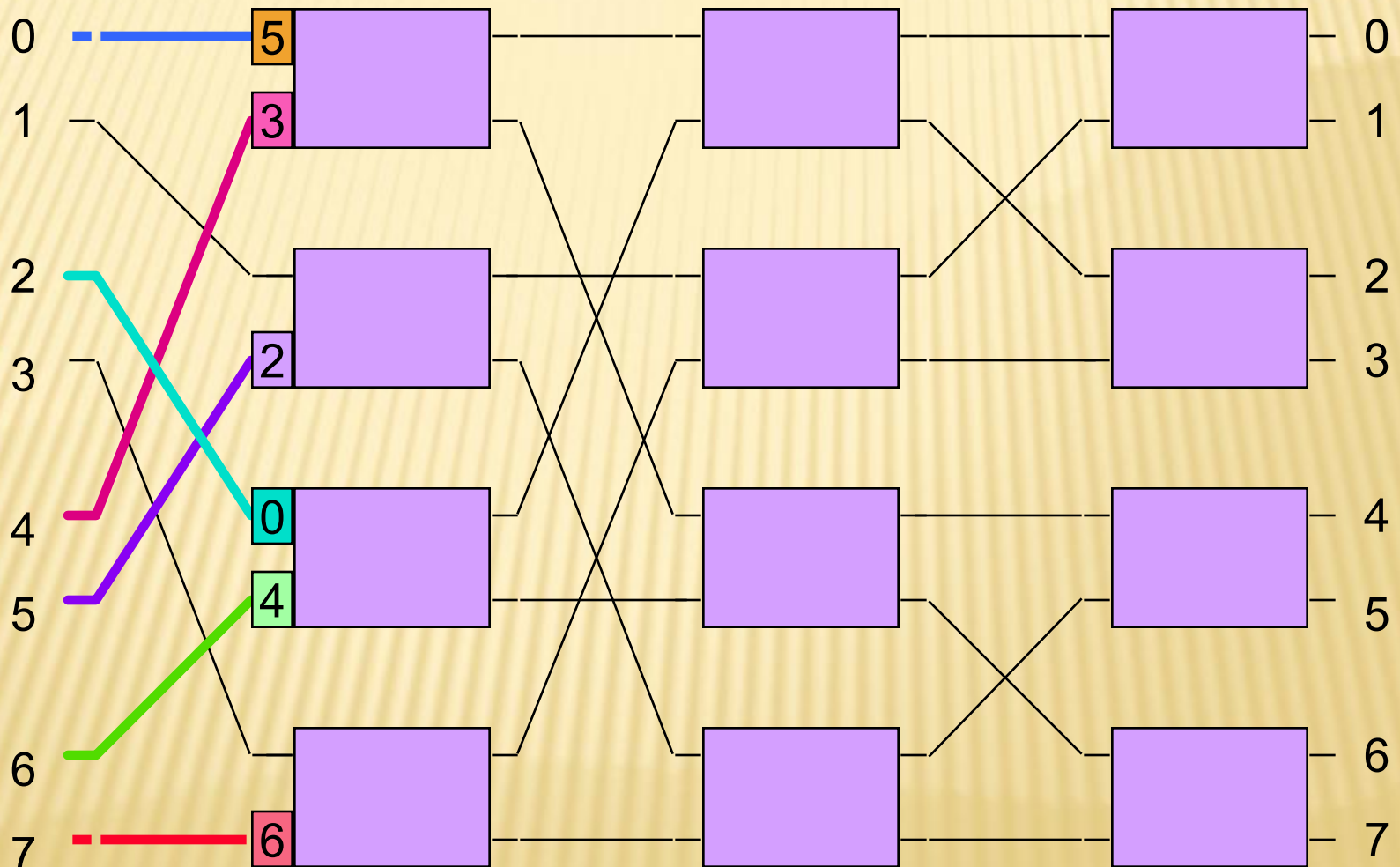
Cell on input port 4 destined for output port 3



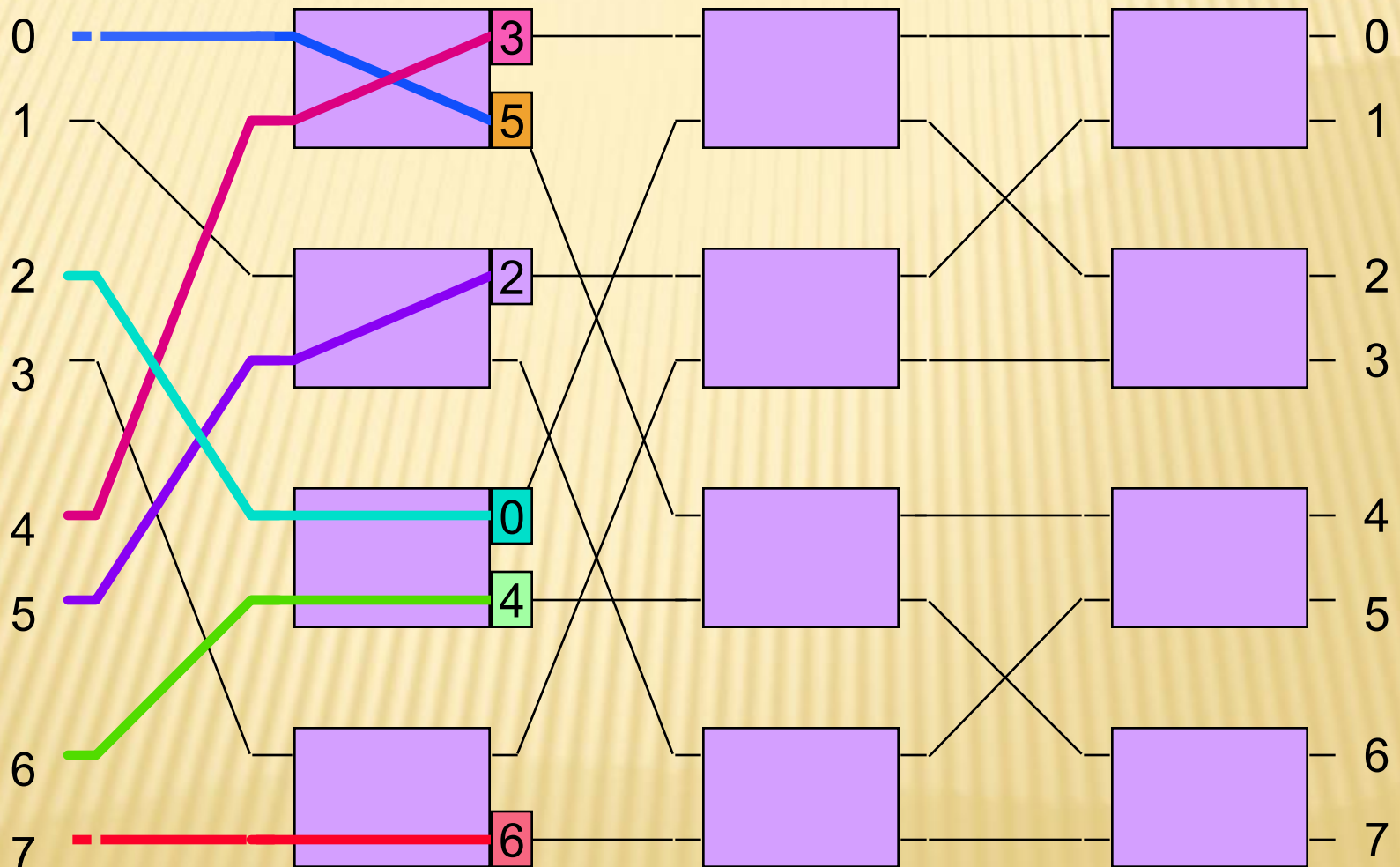
PERFORMANCE DEGRADATION



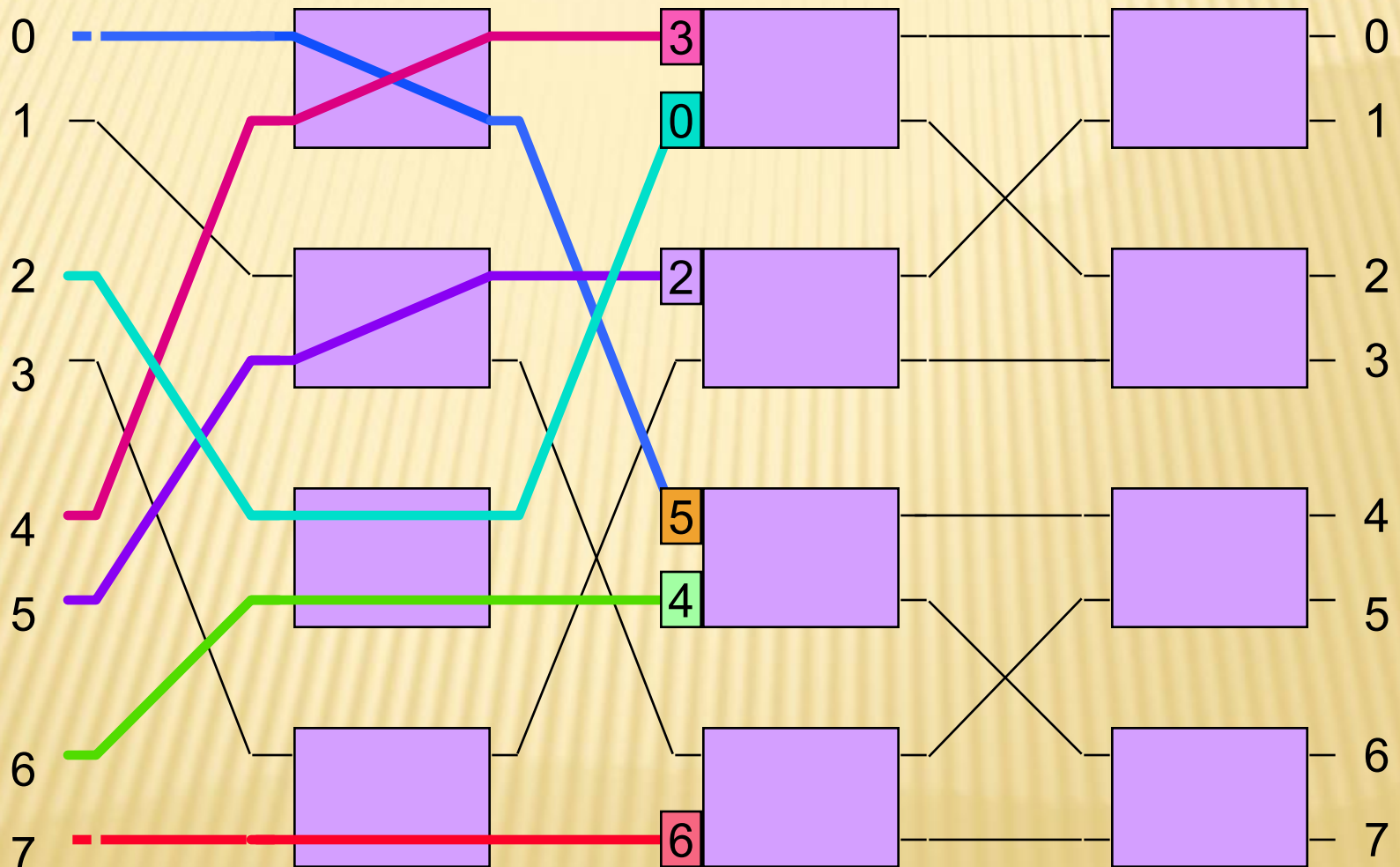
PERFORMANCE DEGRADATION



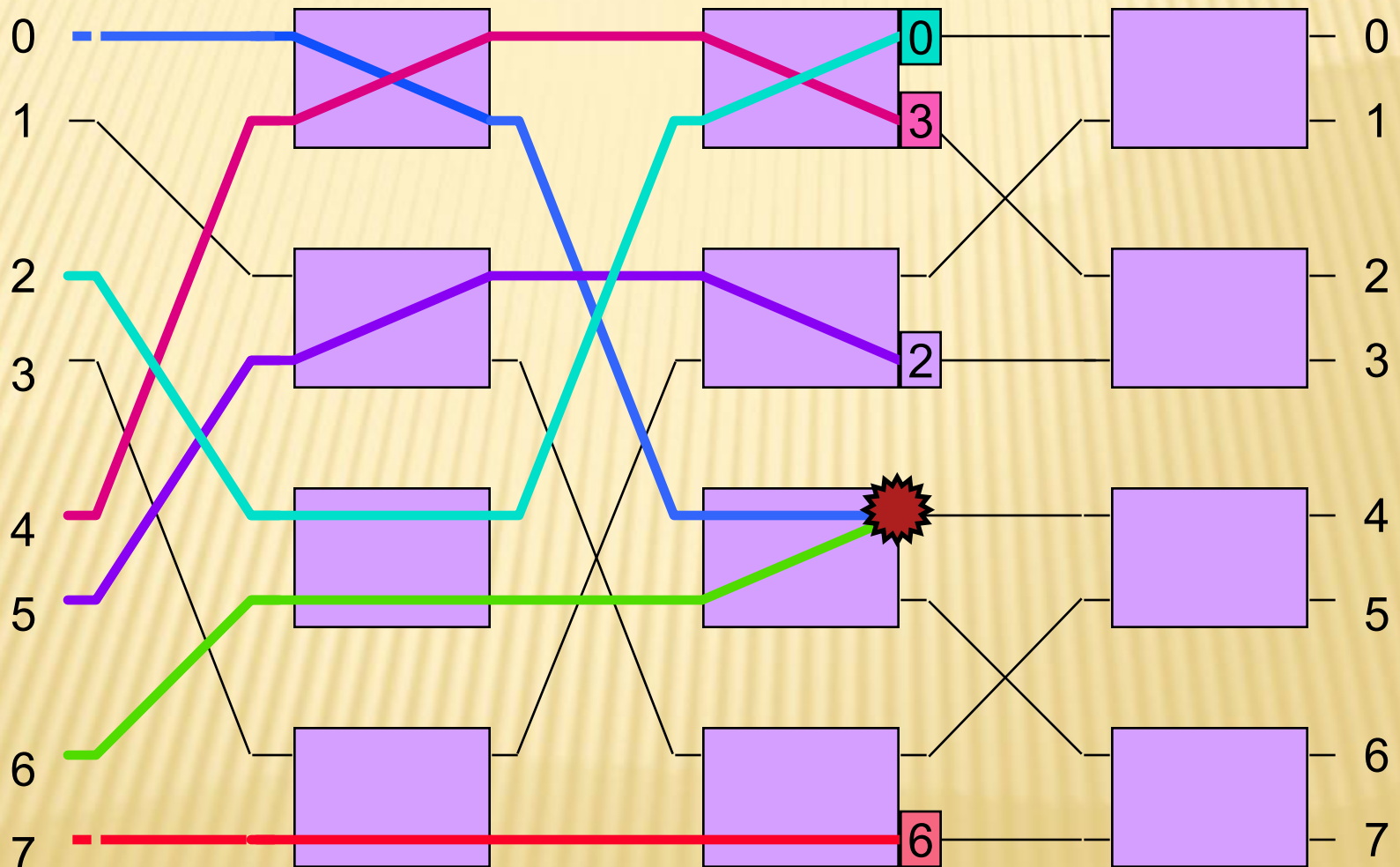
PERFORMANCE DEGRADATION



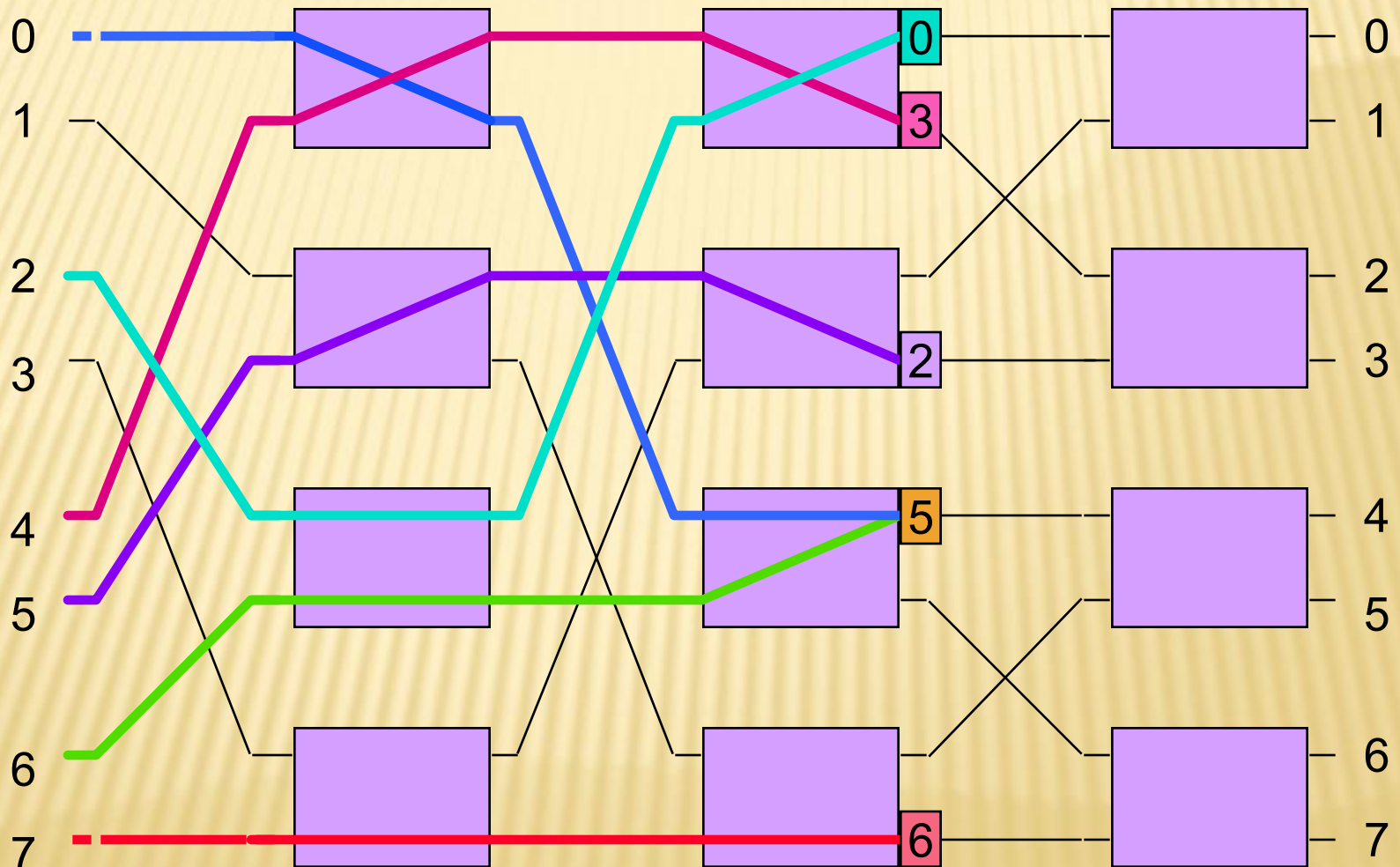
PERFORMANCE DEGRADATION



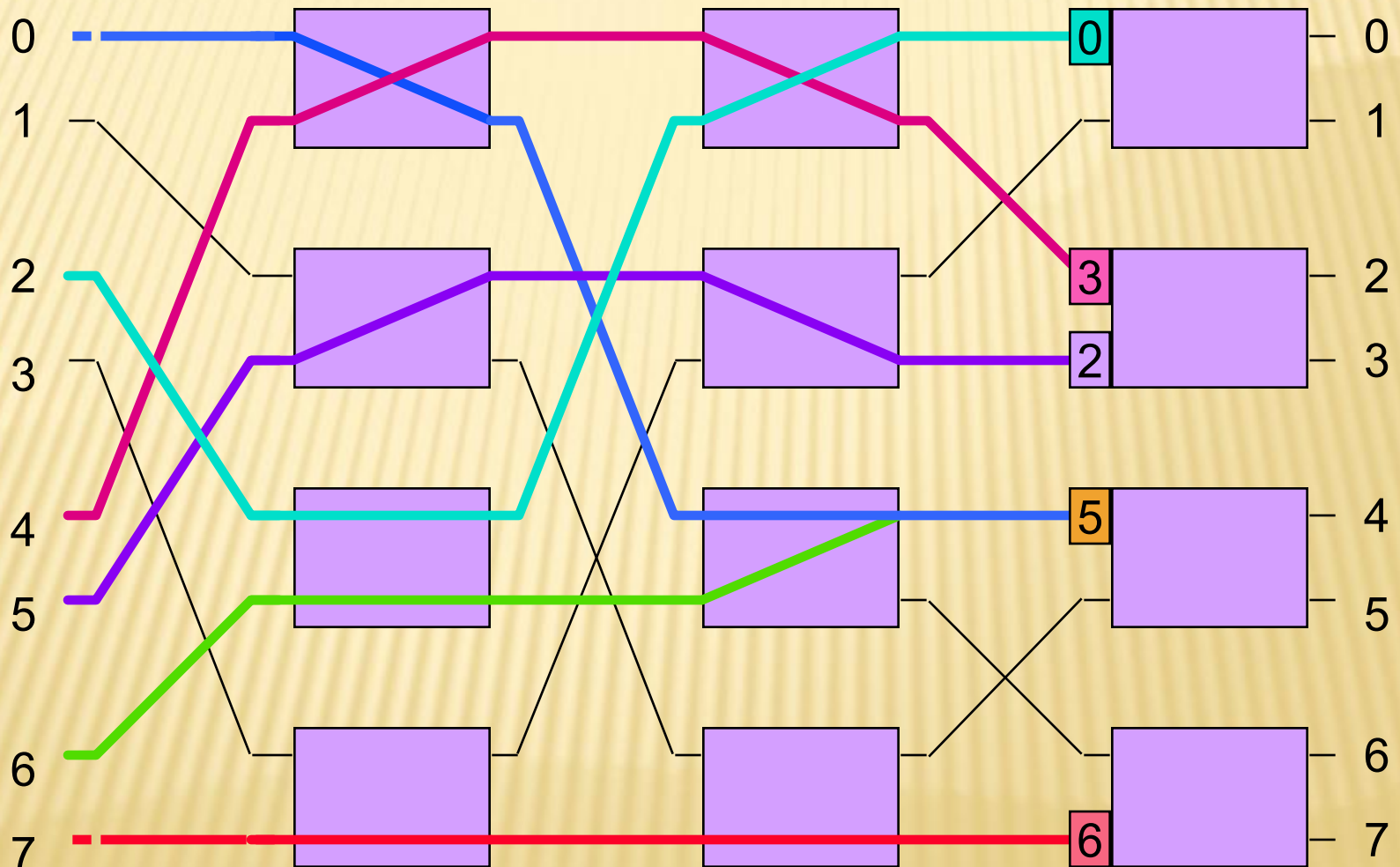
PERFORMANCE DEGRADATION



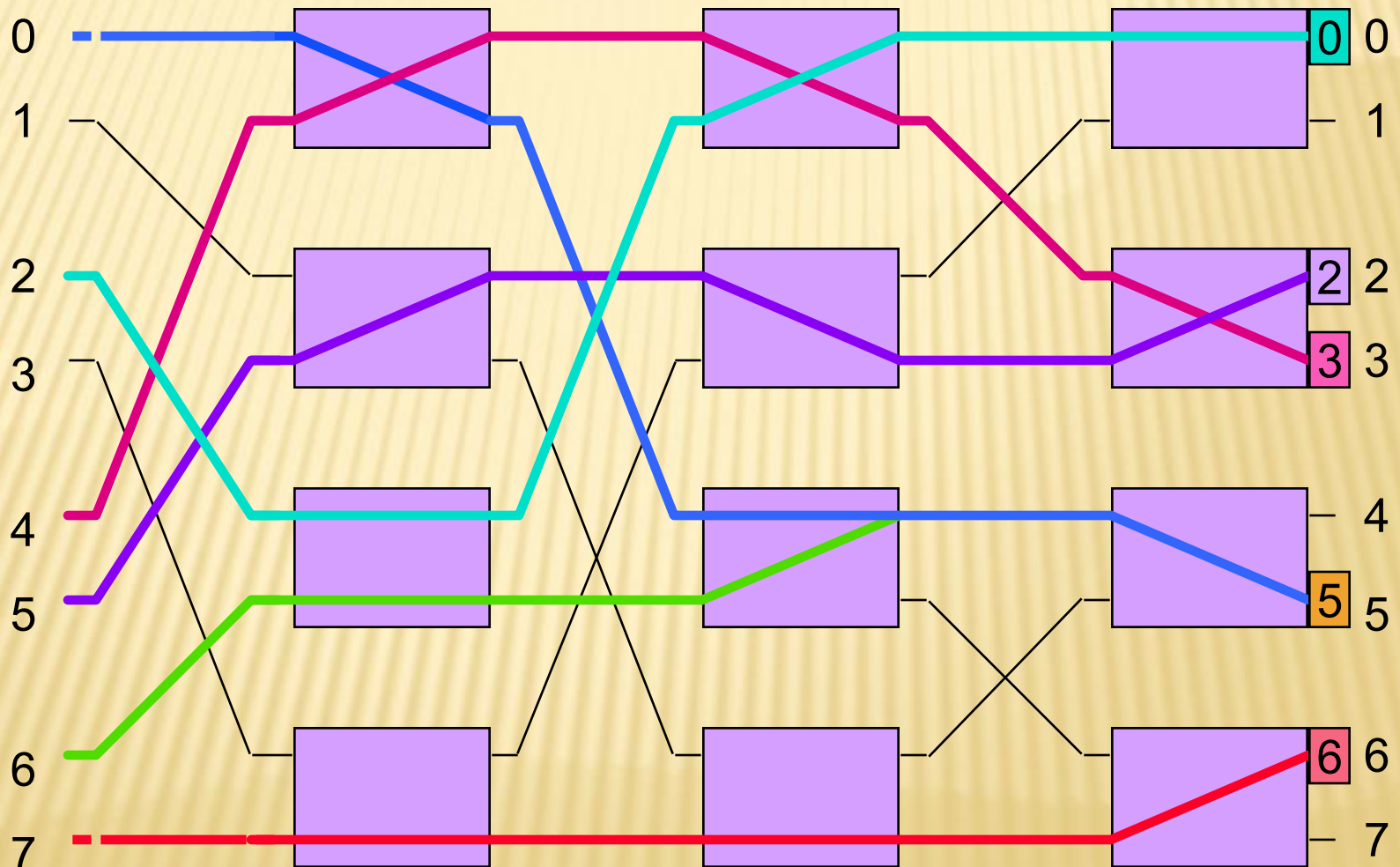
PERFORMANCE DEGRADATION



PERFORMANCE DEGRADATION



PERFORMANCE DEGRADATION



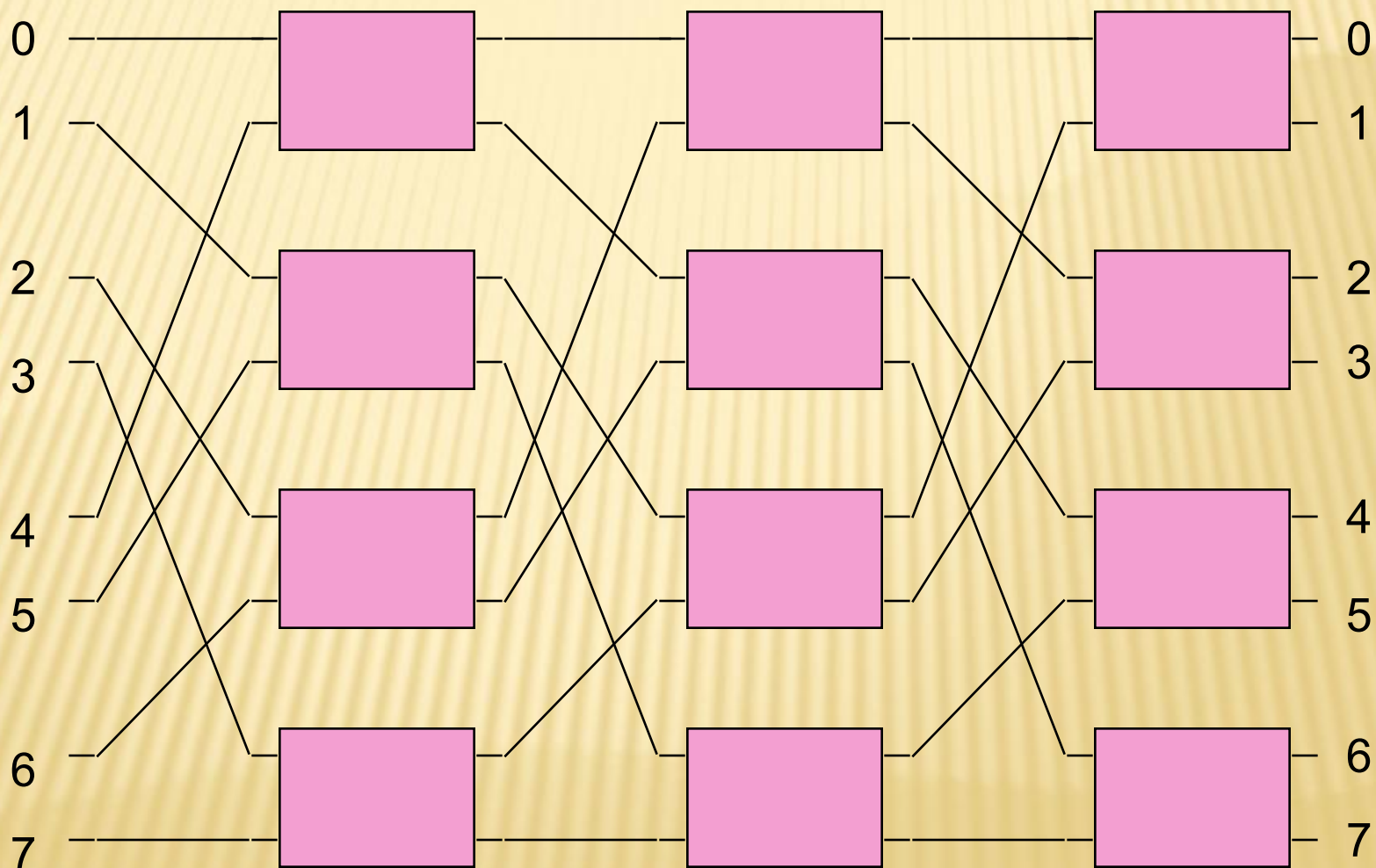
OMEGA NETWORK

- The omega network is another example of a banyan multistage interconnection network that can be used as a switch fabric
- The omega differs from the delta network in the pattern of interconnections between the stages
- The omega MIN uses the “perfect shuffle”

PERFECT SHUFFLE

- ✗ The interconnections between stages are defined by the logical “rotate left” of the bits used in the port ids
- ✗ Example: 000 ---> 000 ---> 000 ---> 000
- ✗ Example: 001 ---> 010 ---> 100 ---> 001
- ✗ Example: 011 ---> 110 ---> 101 ---> 011
- ✗ Example: 111 ---> 111 ---> 111 ---> 111

8 X 8 OMEGA NETWORK

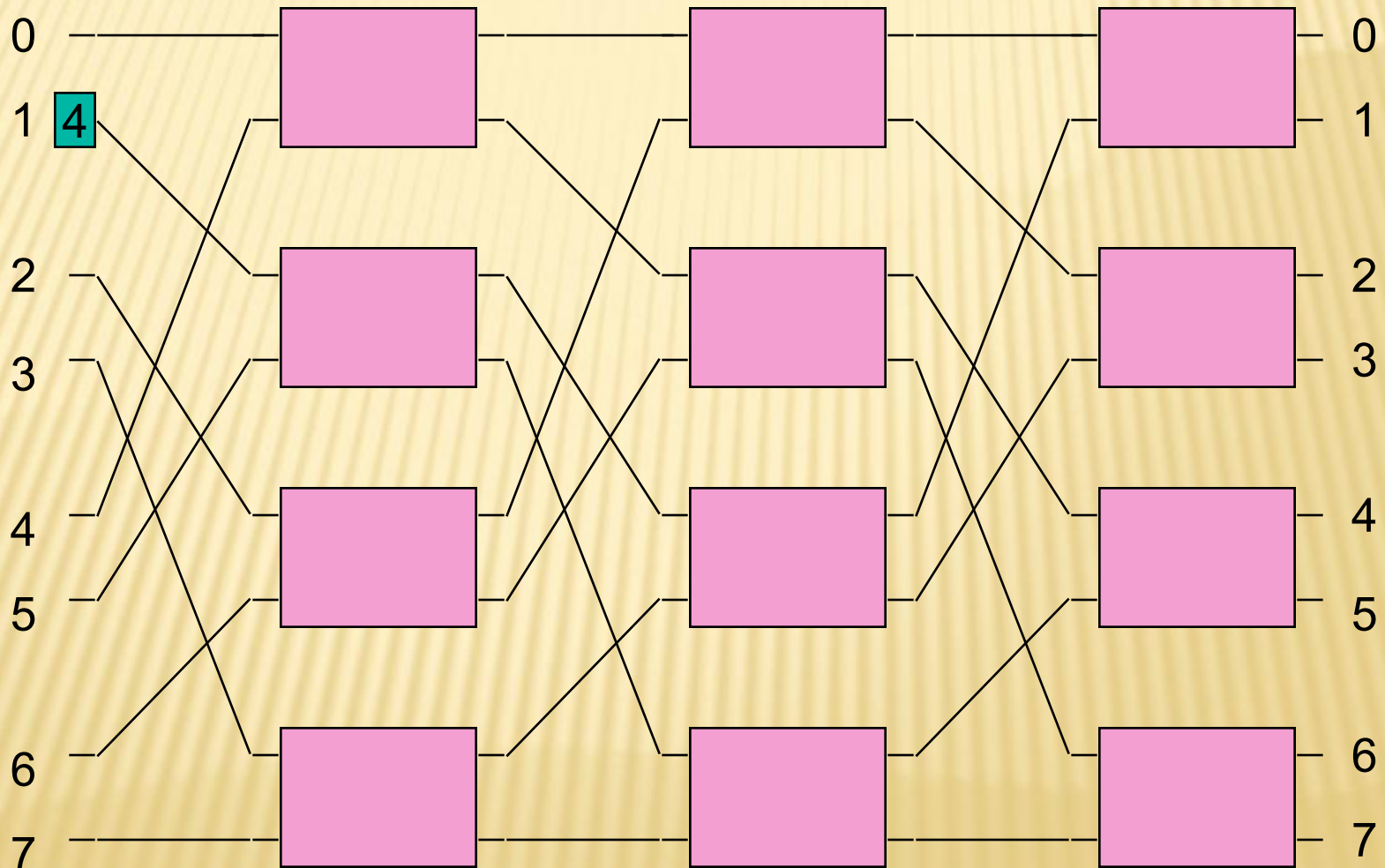


SELF ROUTING

- Omega network has self-routing property
- The path for a cell to reach its destination can be determined directly from its routing tag (i.e., destination port id)
- Stage k of the MIN looks at bit k of the tag
- If bit k is 0, then send cell out upper port
- If bit k is 1, then send cell out lower port
- Works for every possible input port (really!)

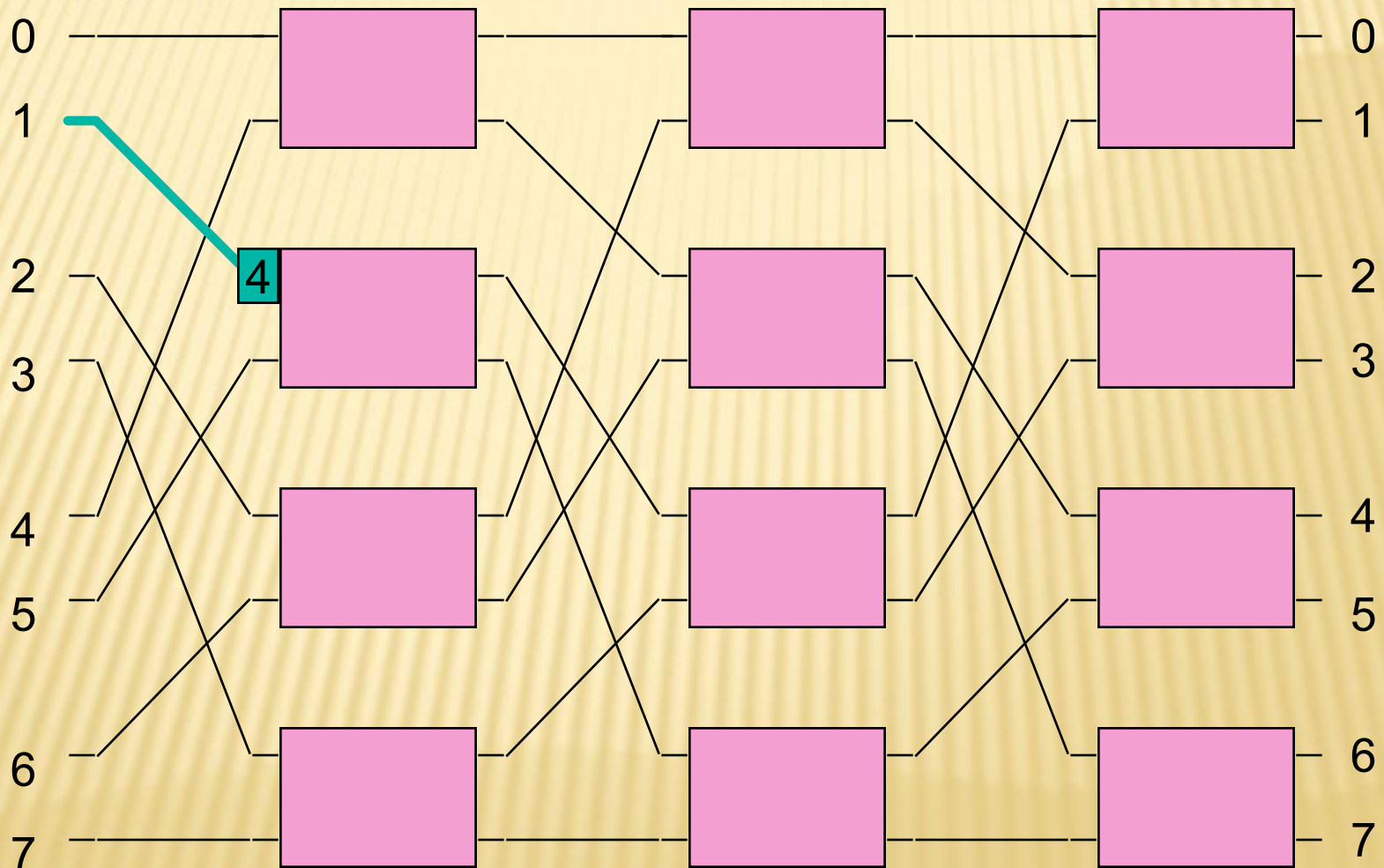
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



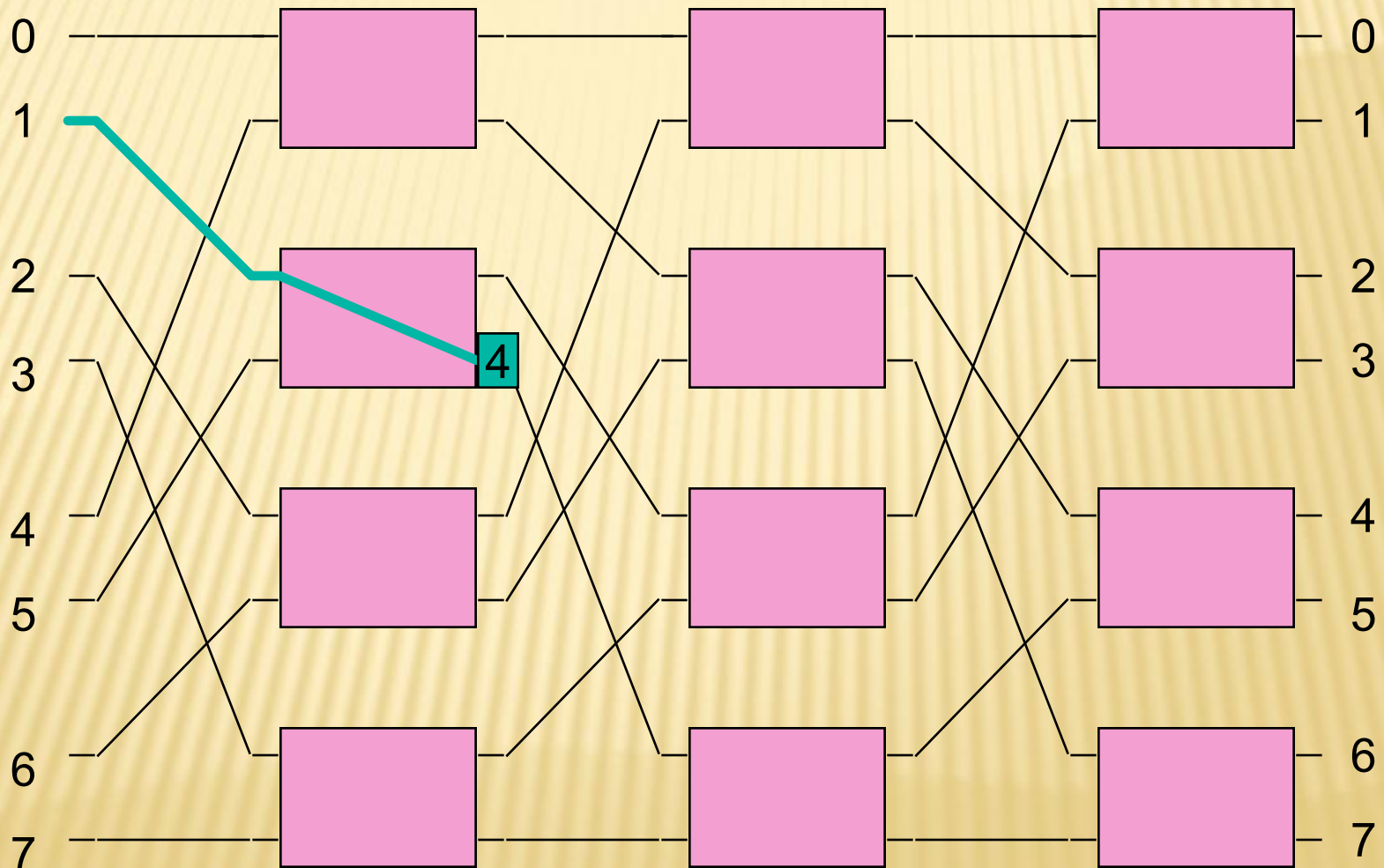
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



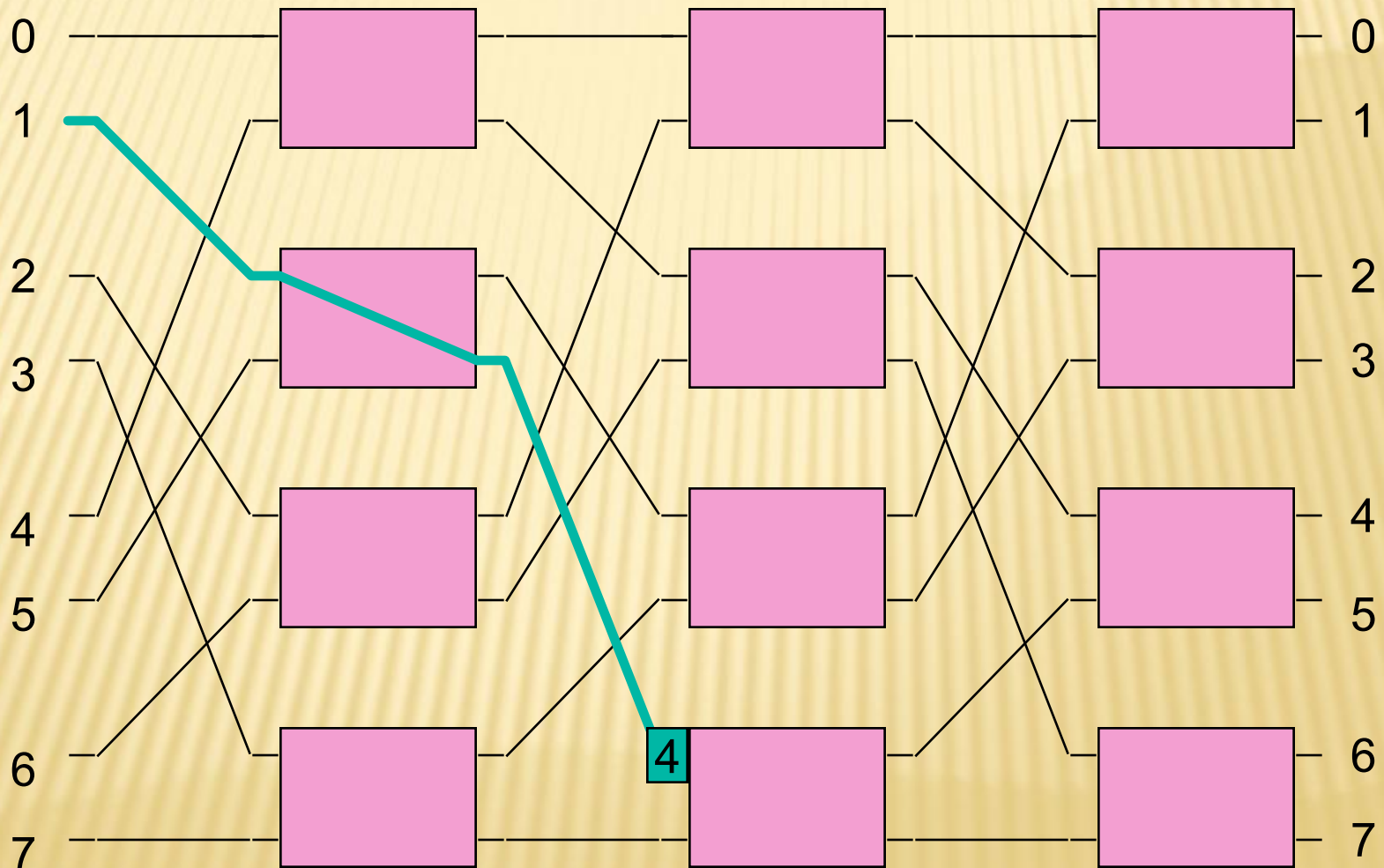
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



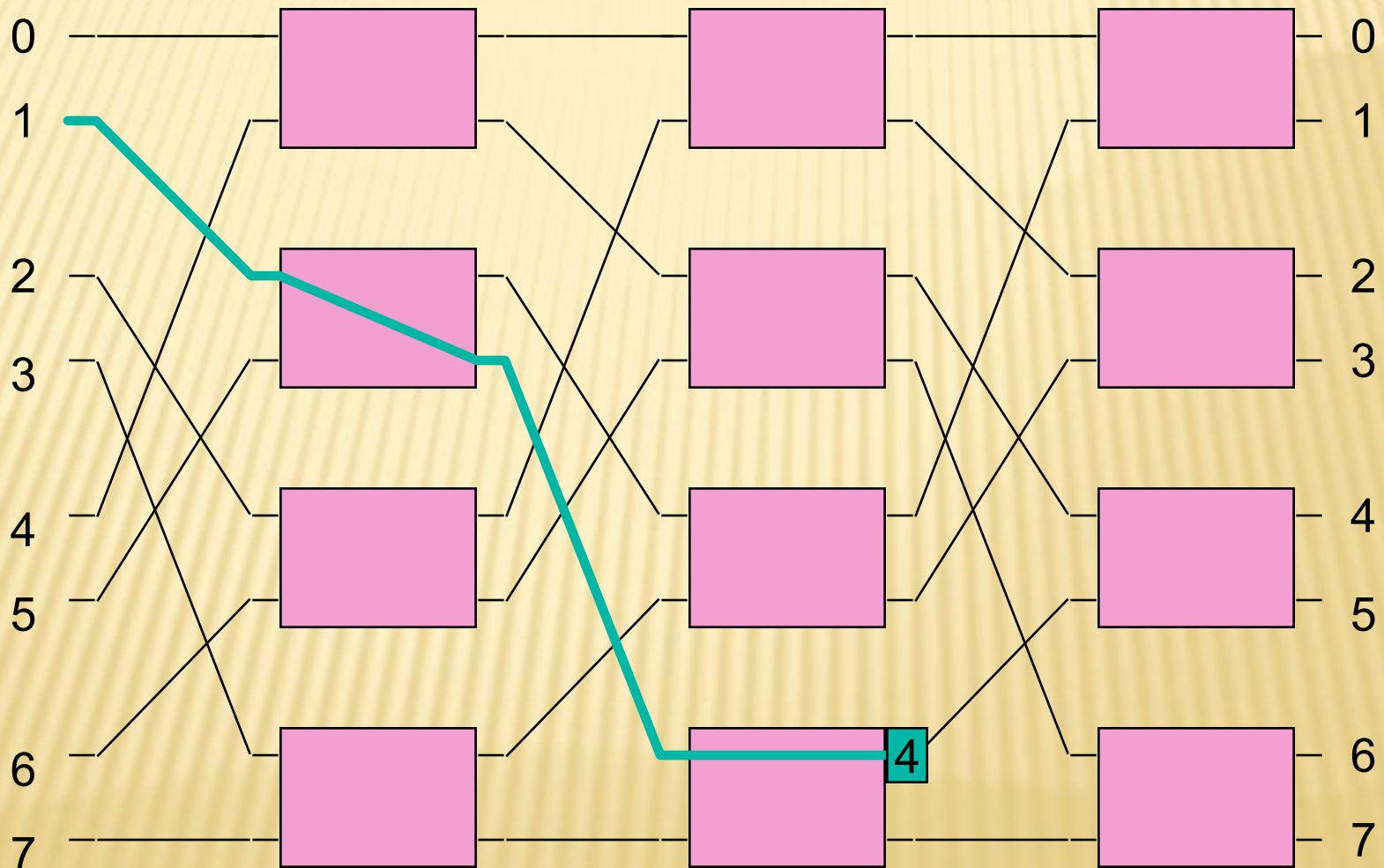
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



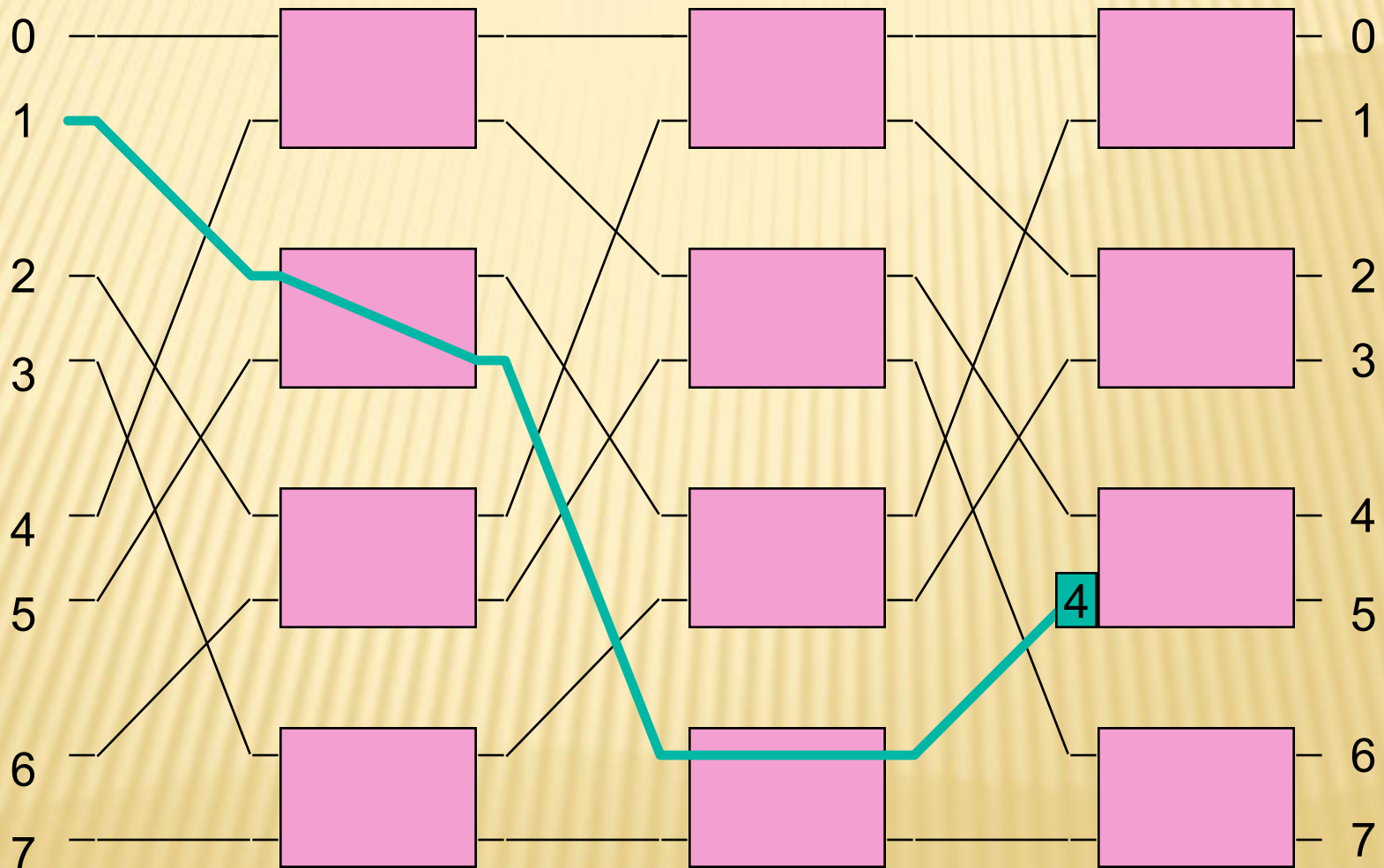
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



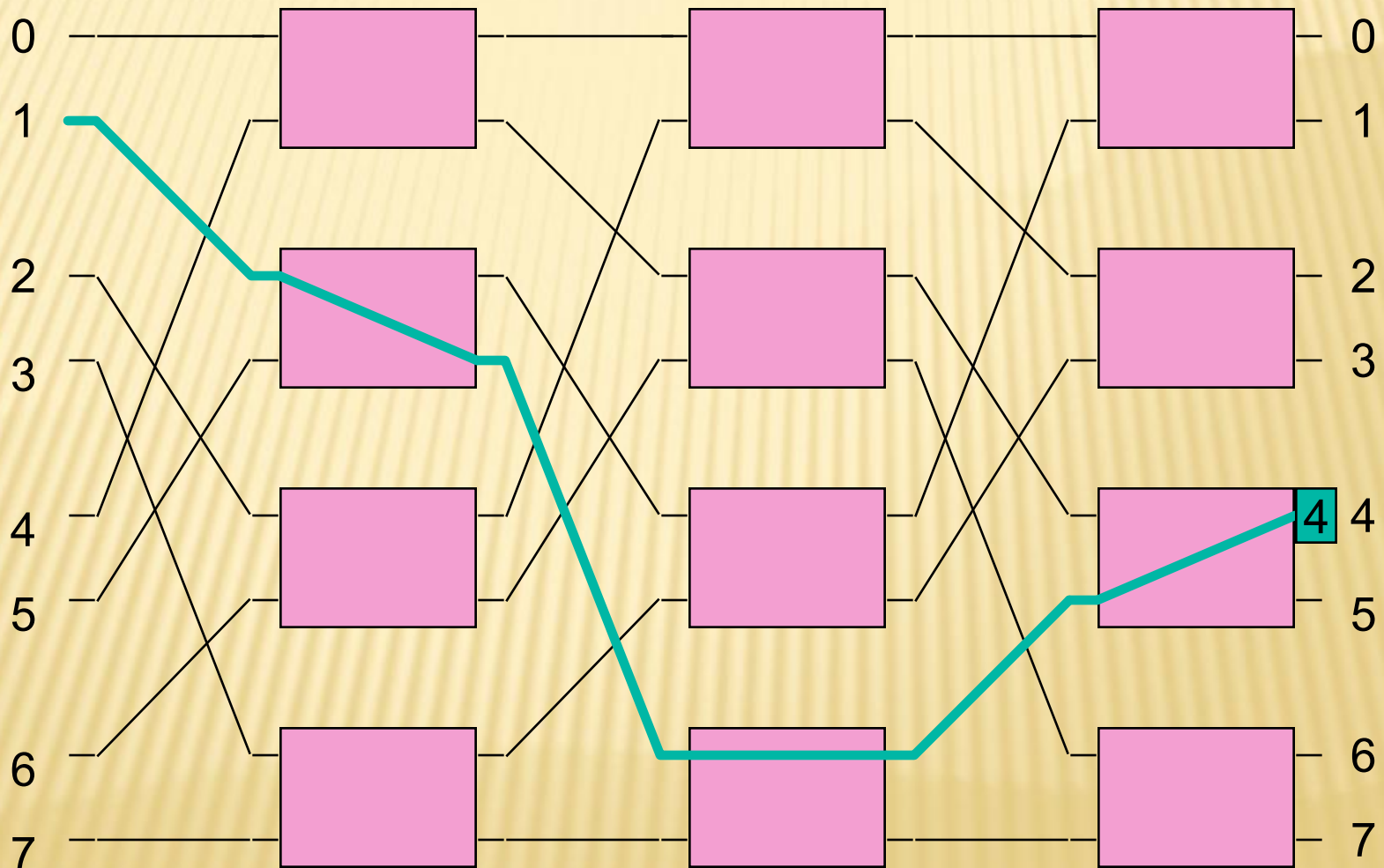
Example of Self Routing

Cell destined for output port 4 ($= 100_2$)



Example of Self Routing

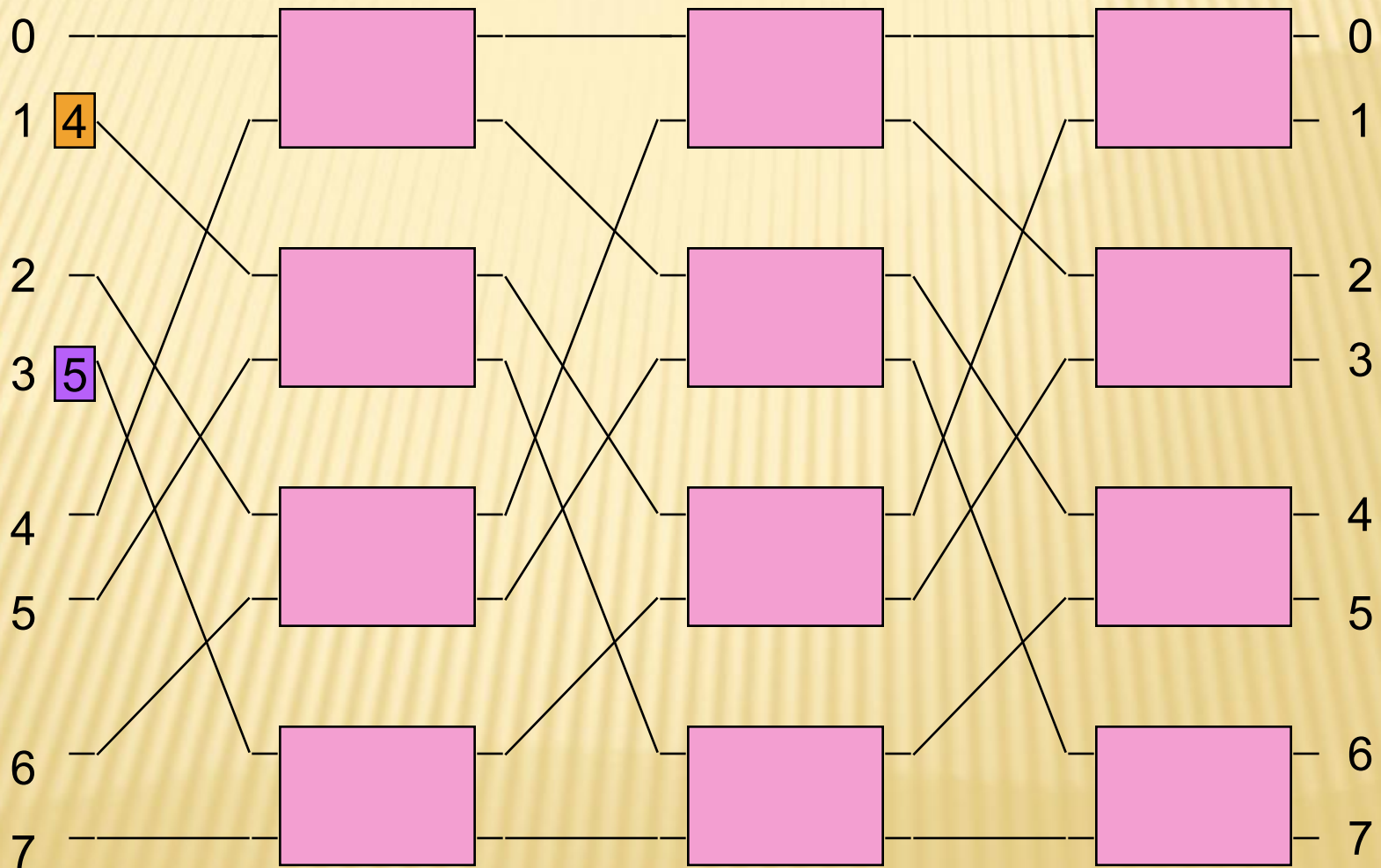
Cell destined for output port 4 ($= 100_2$)



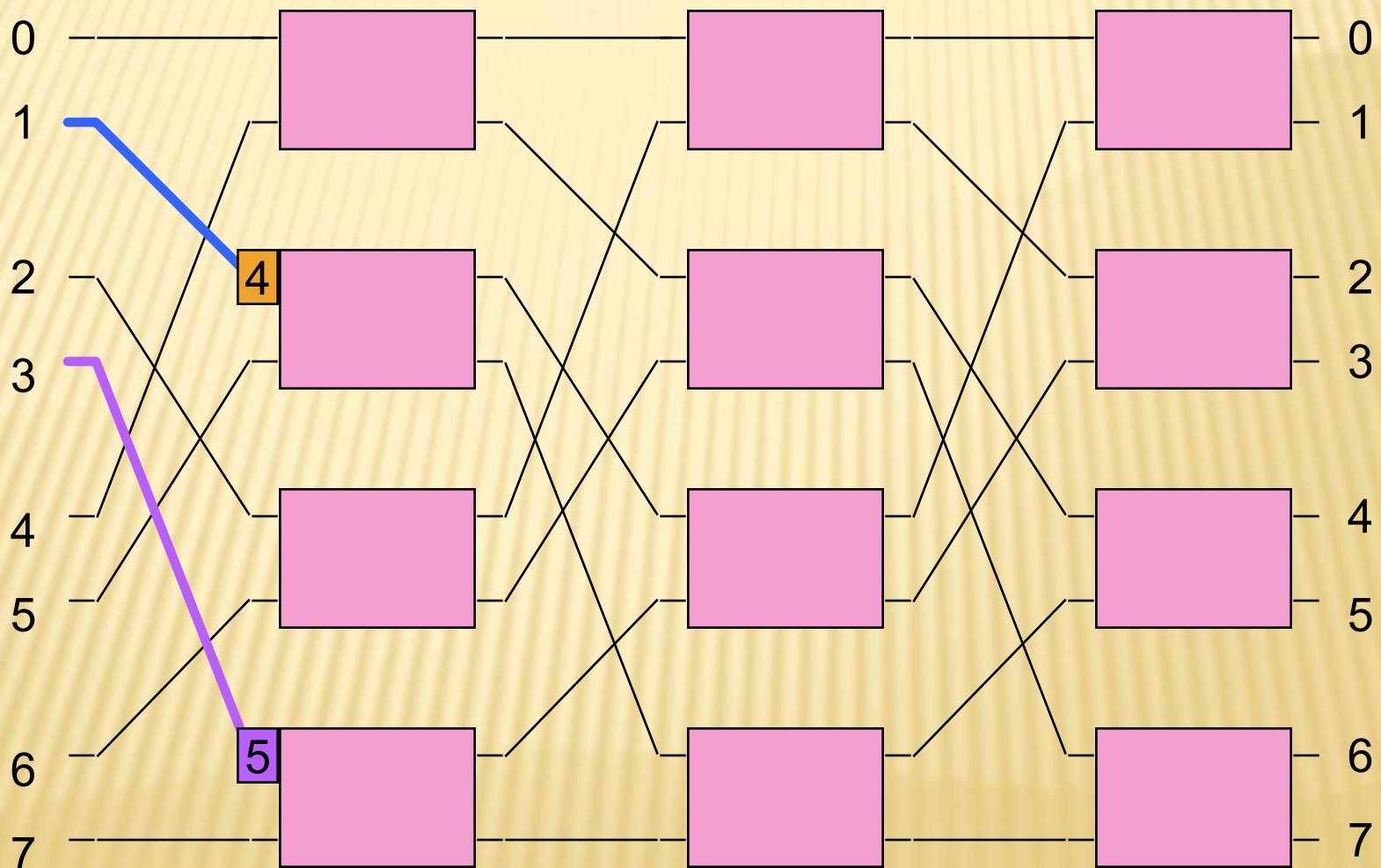
PATH CONTENTION

- ✗ The omega network has the problems as the delta network with output port contention and path contention
- ✗ Again, the result in a bufferless switch fabric is cell loss (one cell wins, one loses)
- ✗ Path contention and output port contention can seriously degrade the achievable throughput of the switch

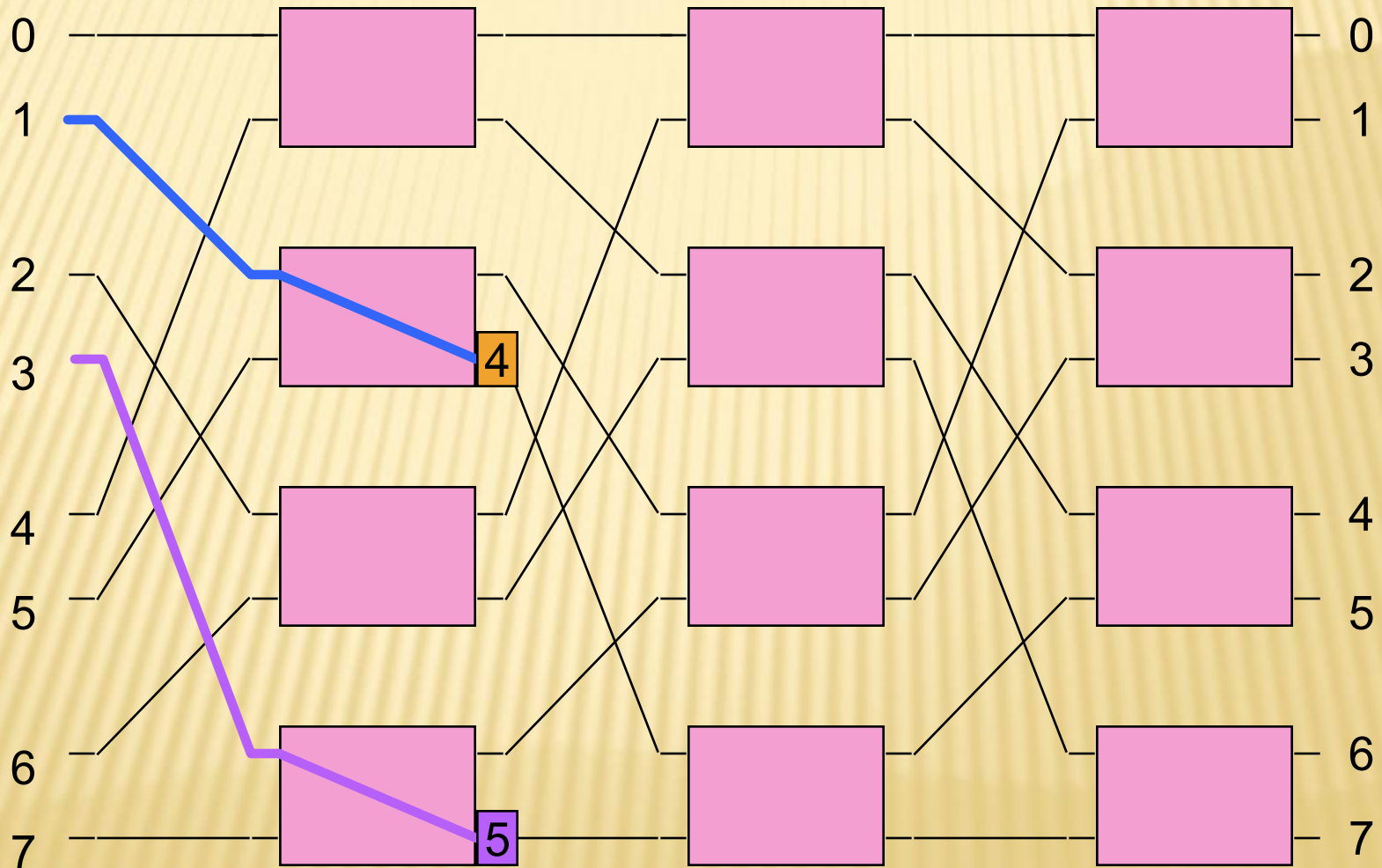
Path Contention



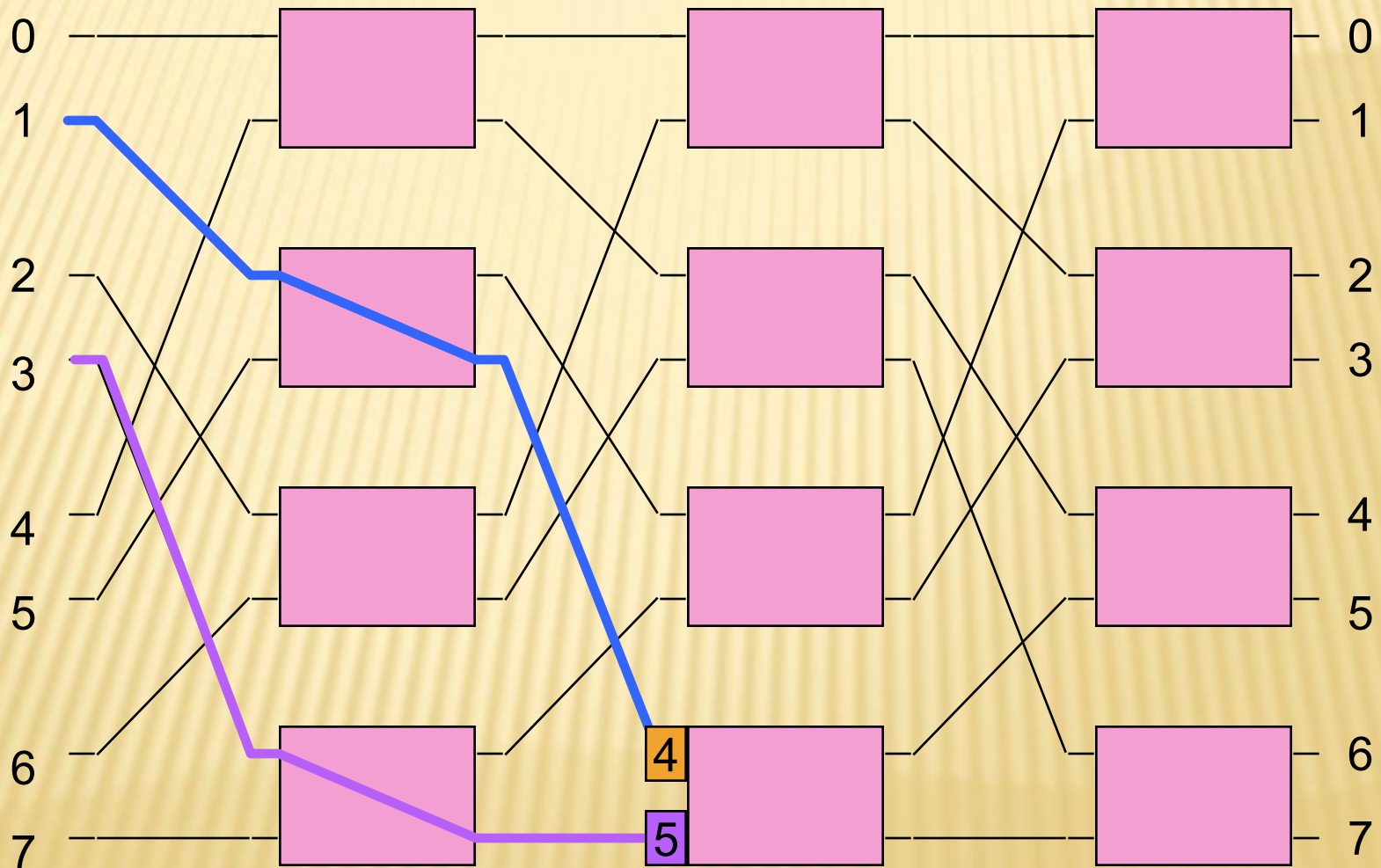
Path Contention



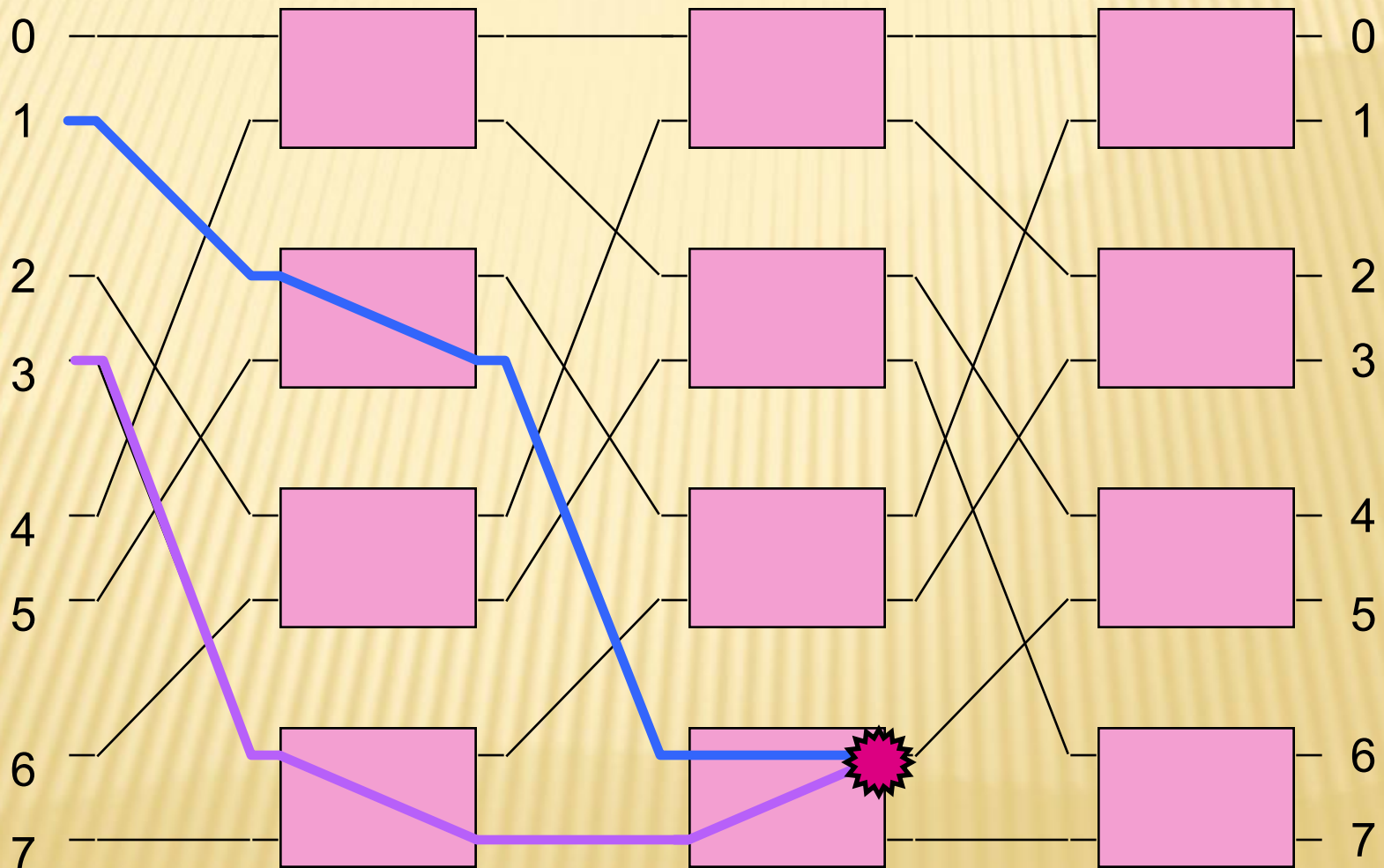
Path Contention



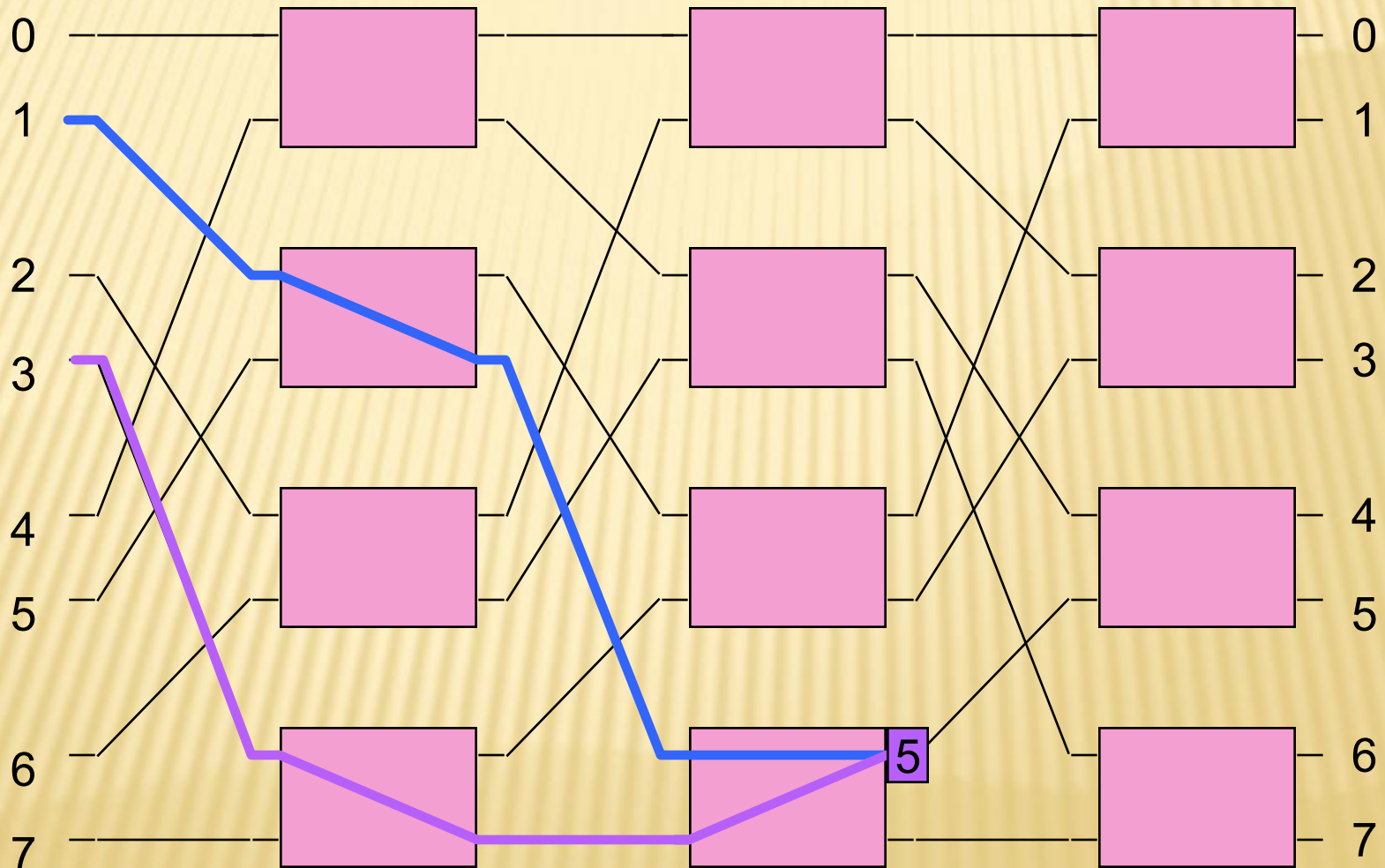
Path Contention



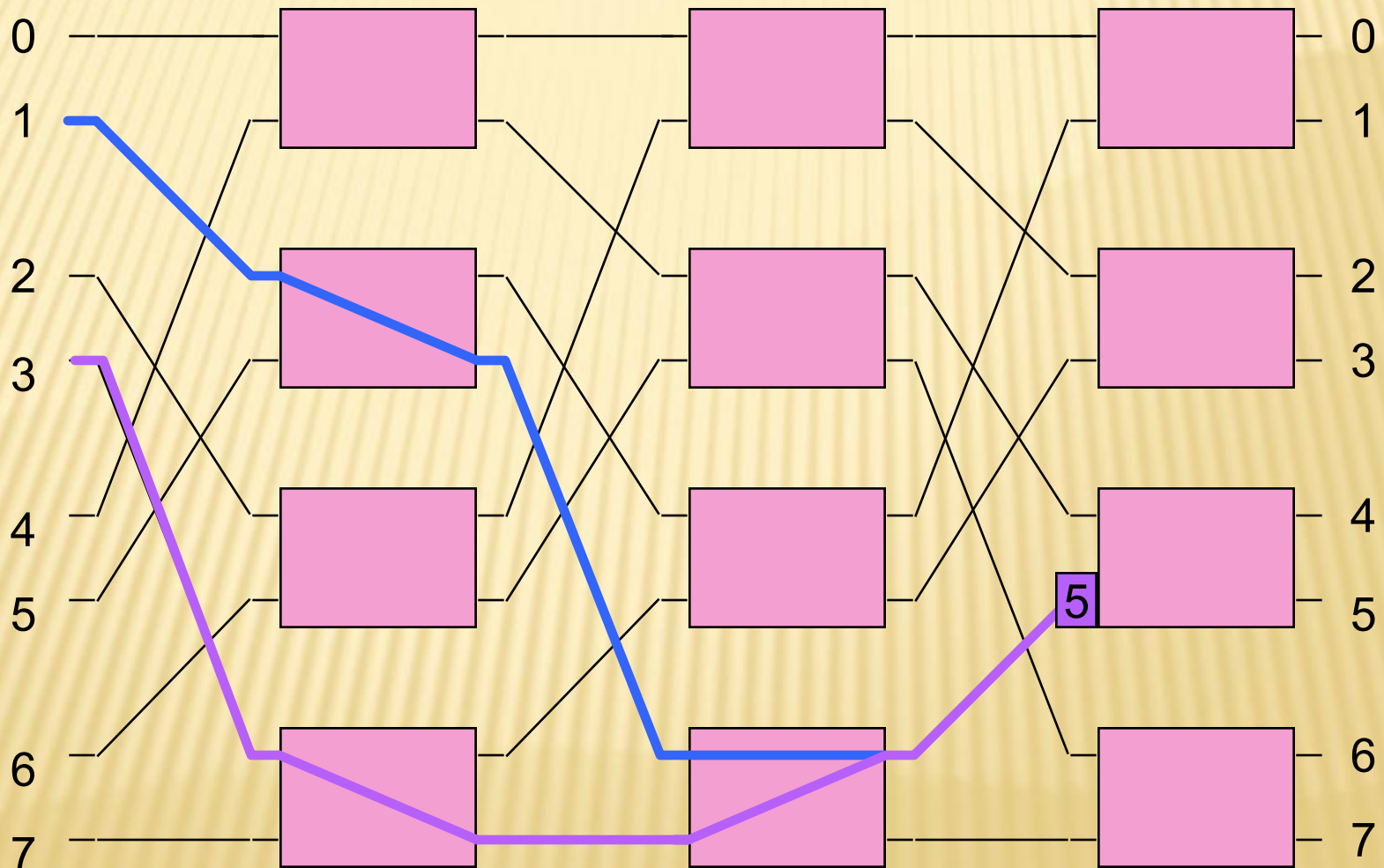
Path Contention



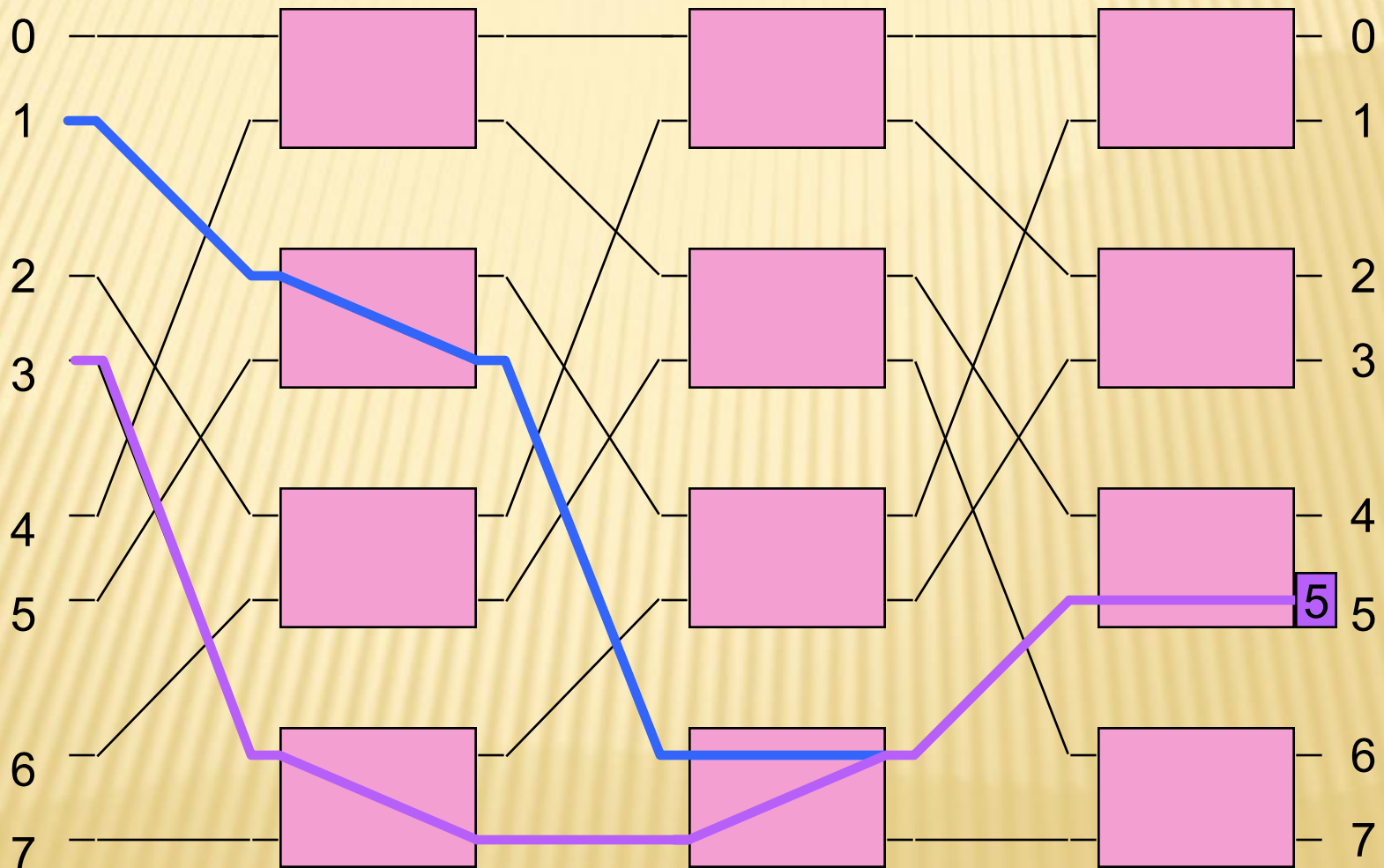
Path Contention



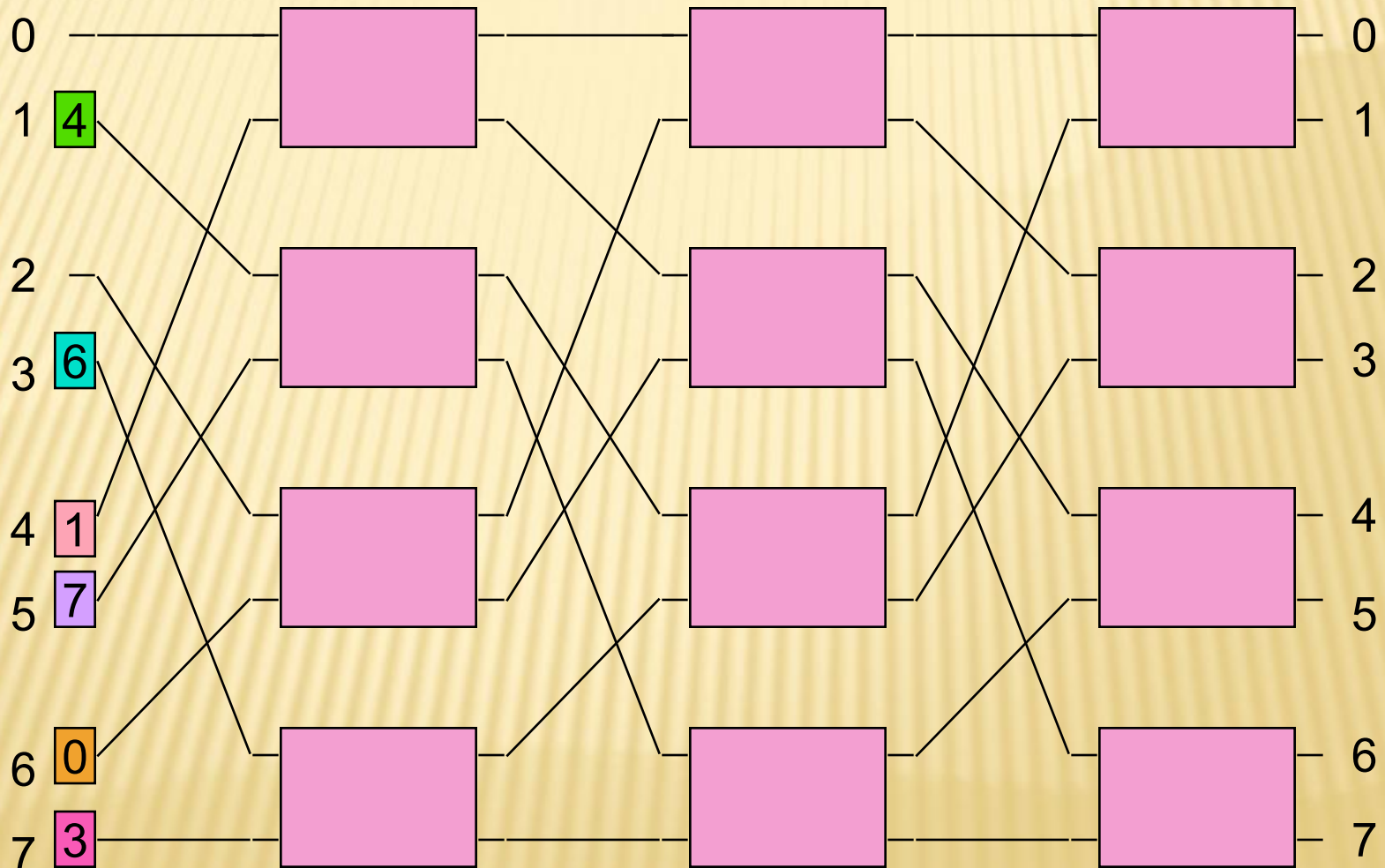
Path Contention



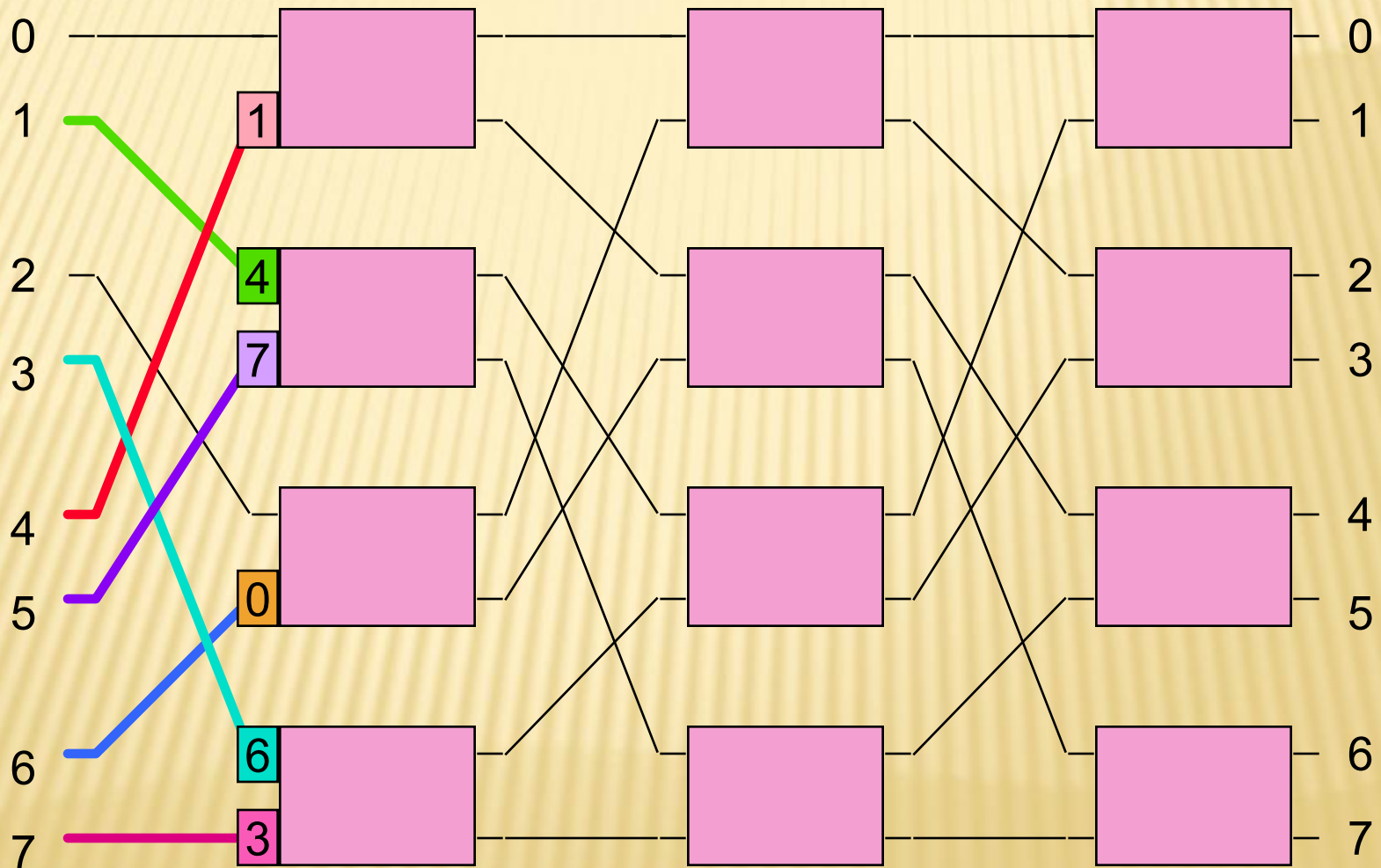
Path Contention



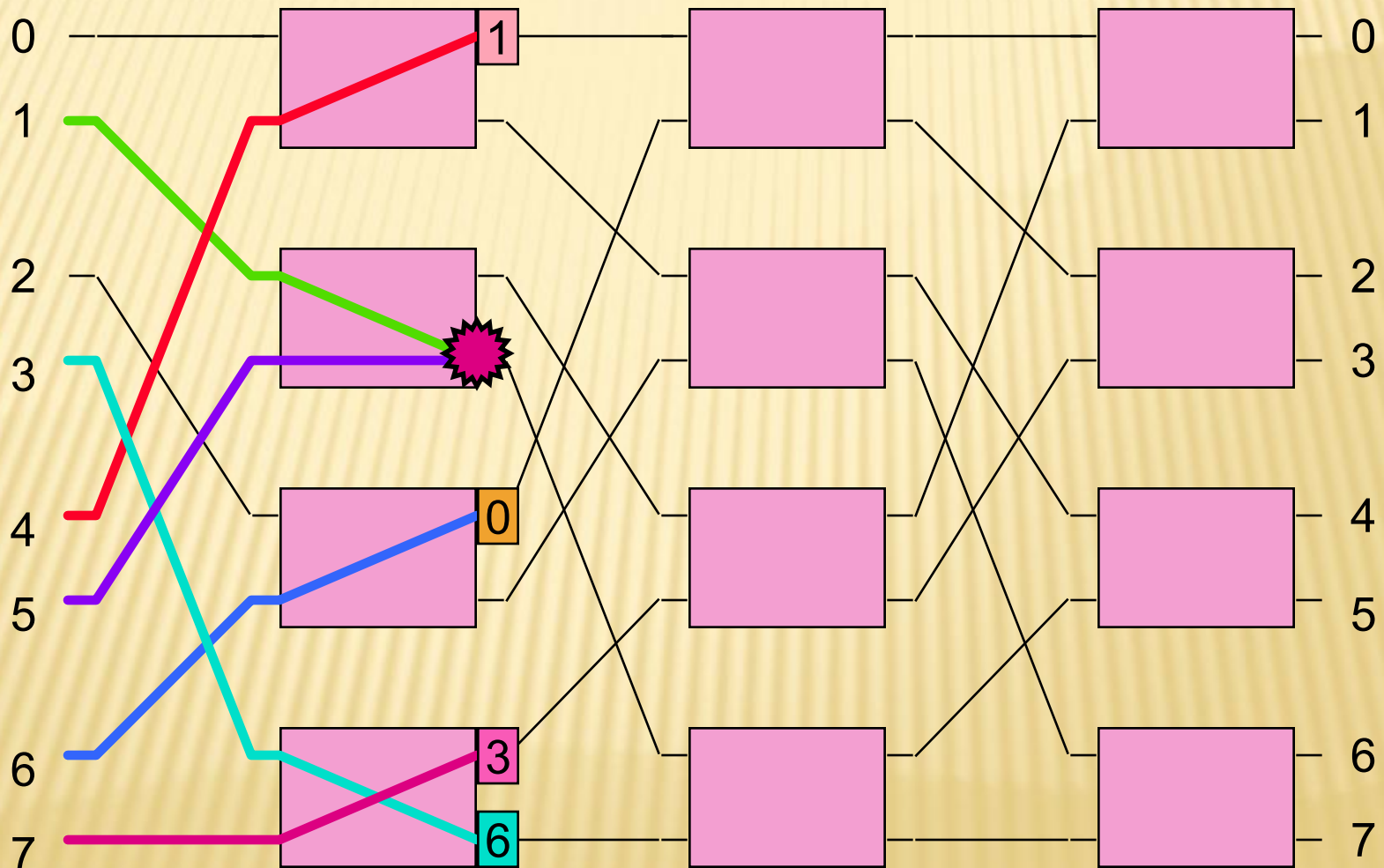
PERFORMANCE DEGRADATION



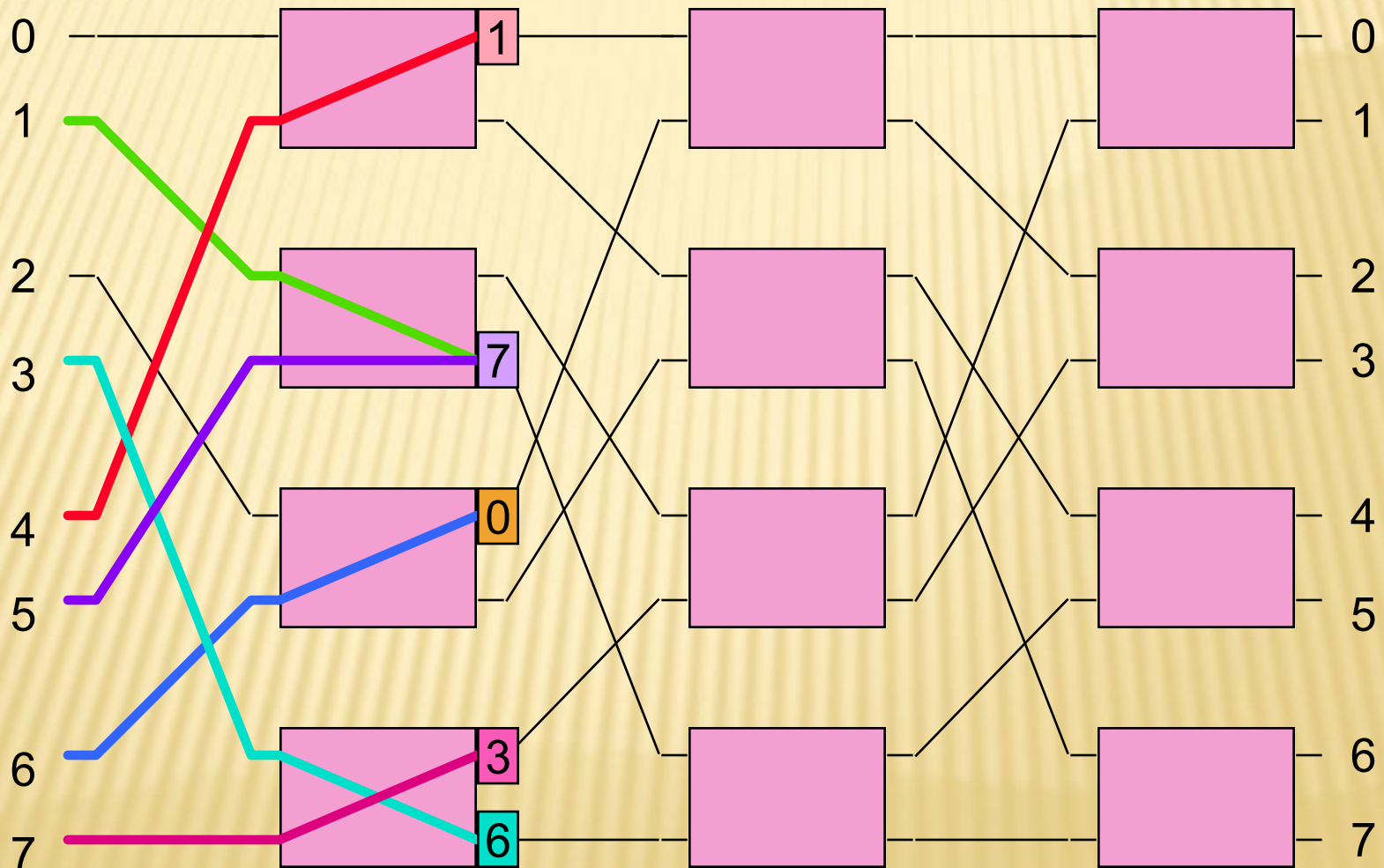
PERFORMANCE DEGRADATION



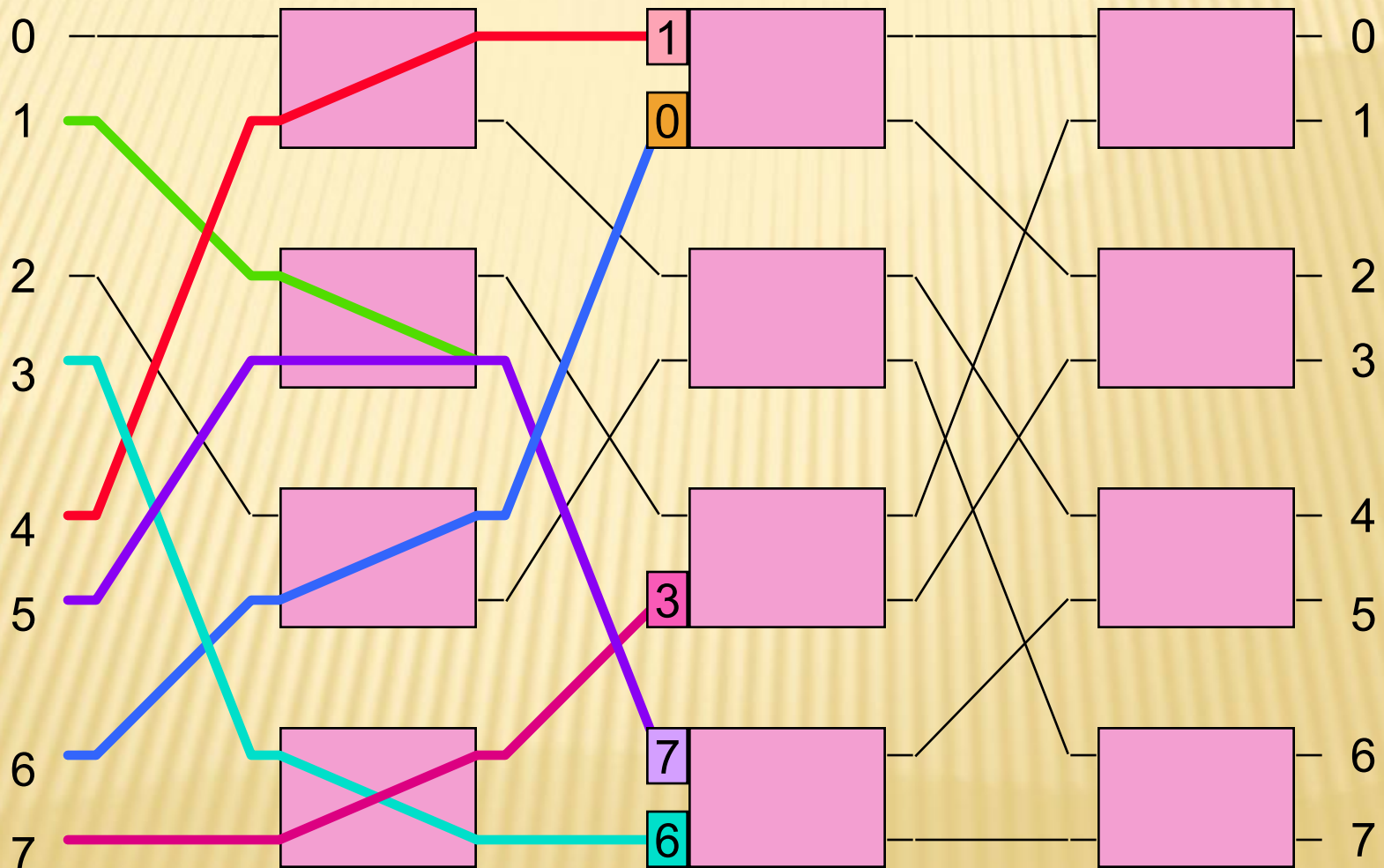
PERFORMANCE DEGRADATION



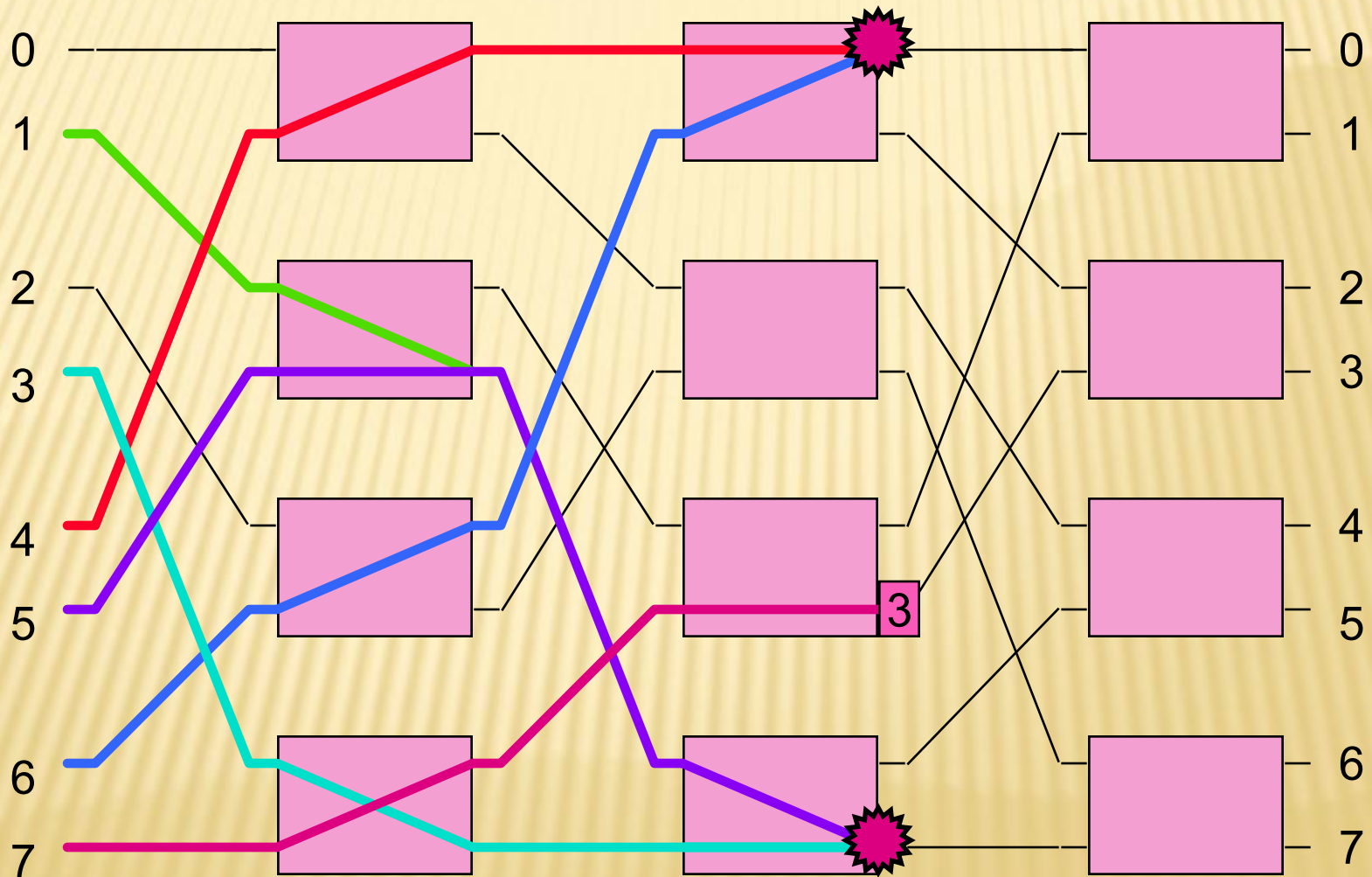
PERFORMANCE DEGRADATION



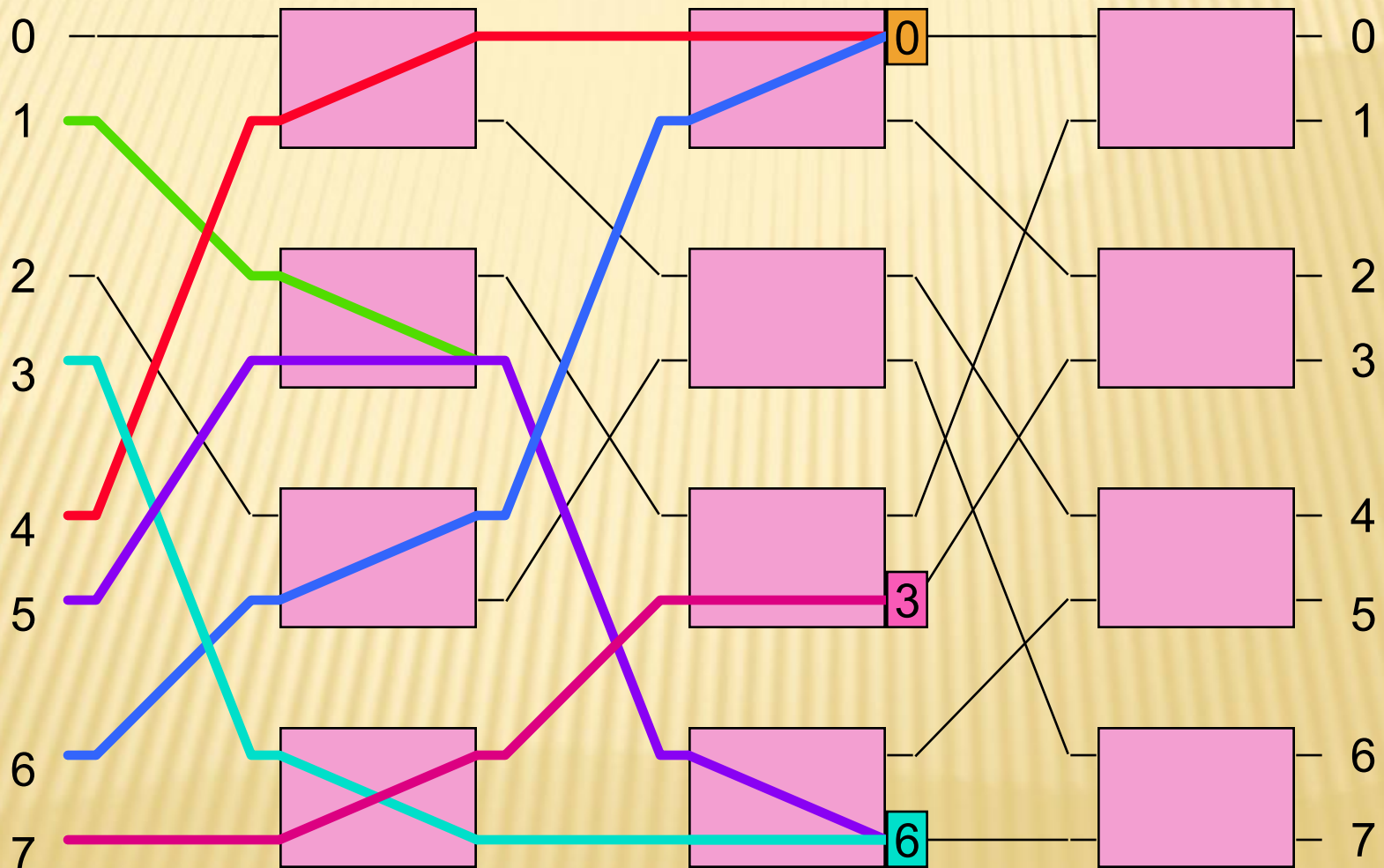
PERFORMANCE DEGRADATION



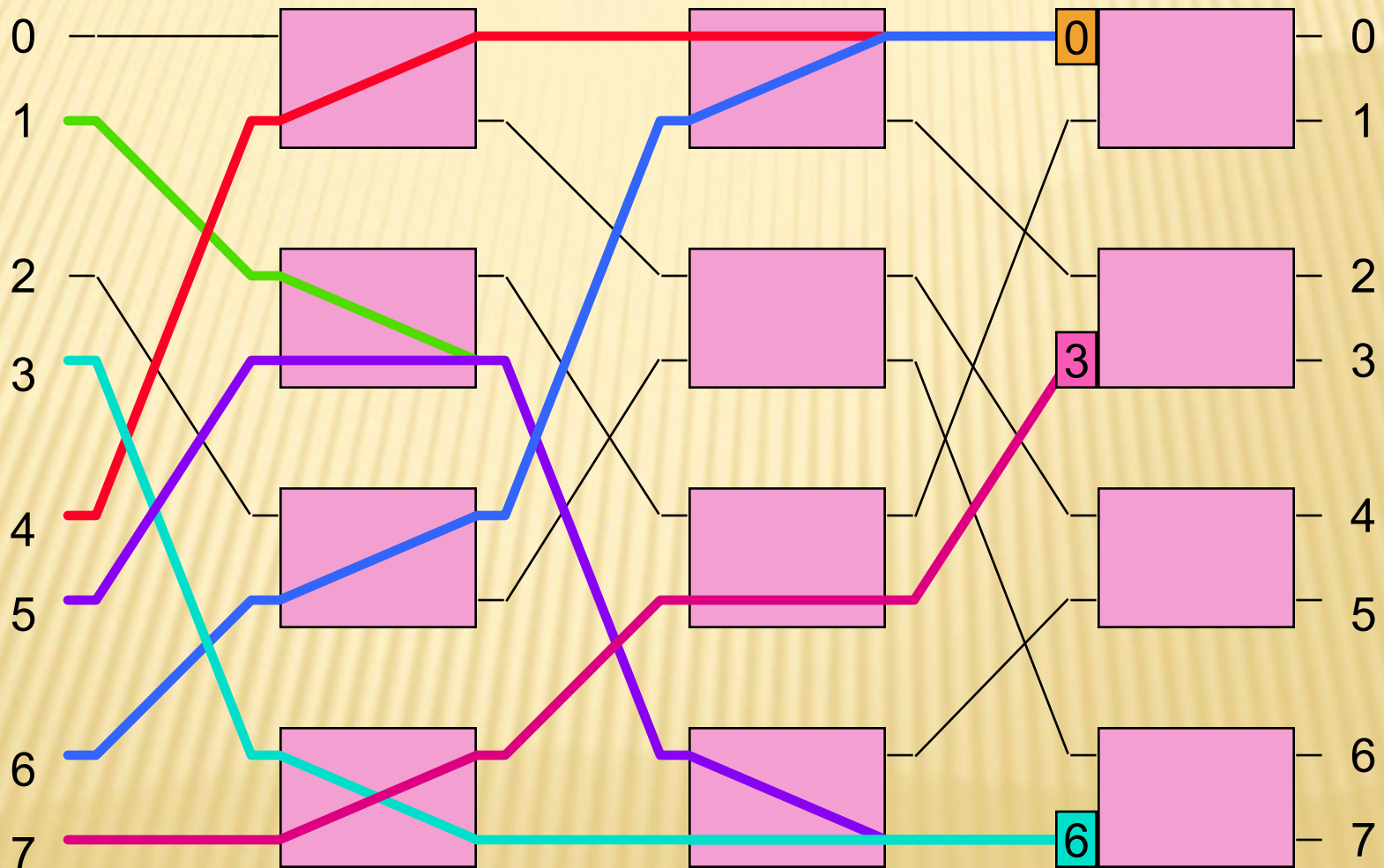
PERFORMANCE DEGRADATION



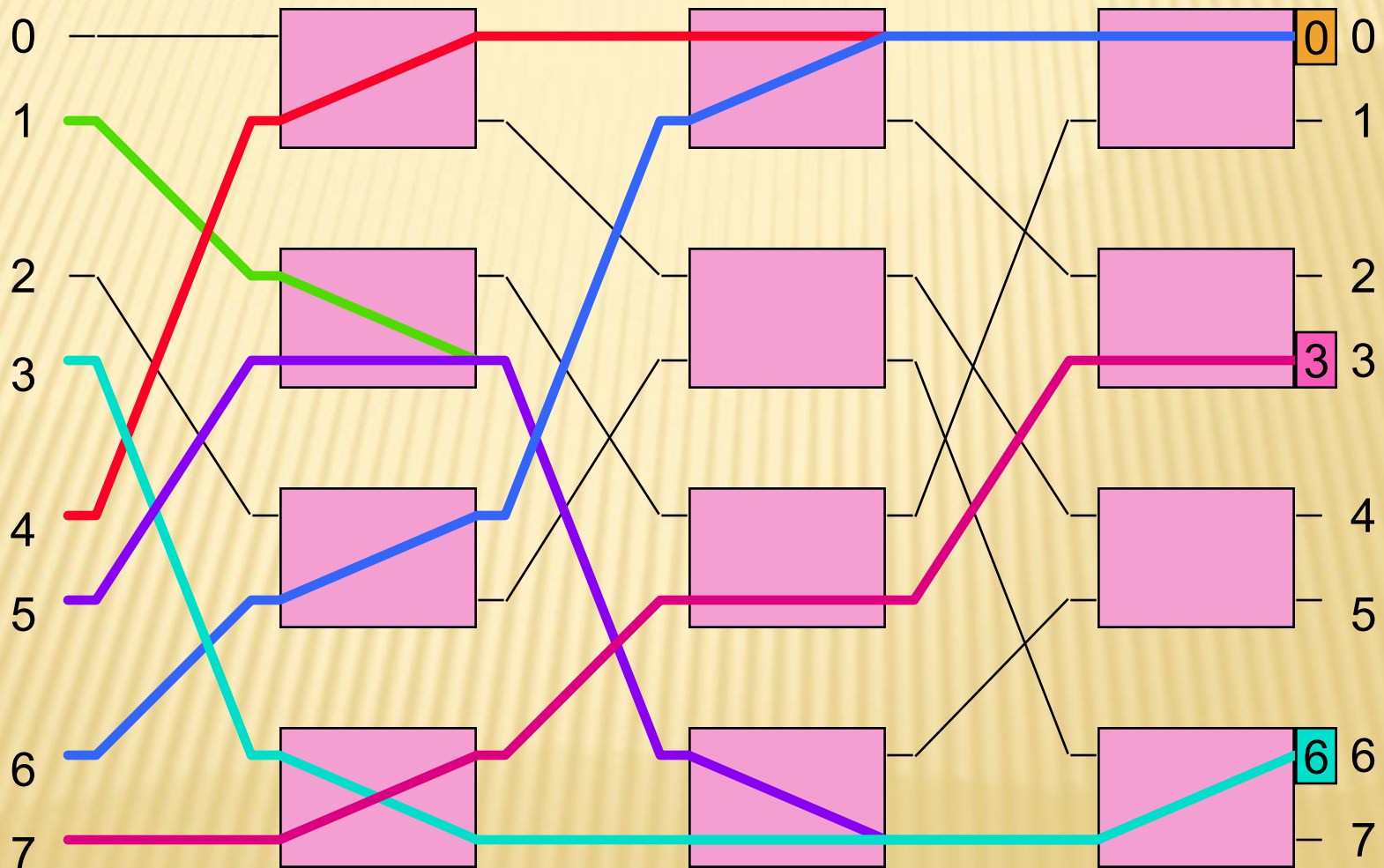
PERFORMANCE DEGRADATION



PERFORMANCE DEGRADATION



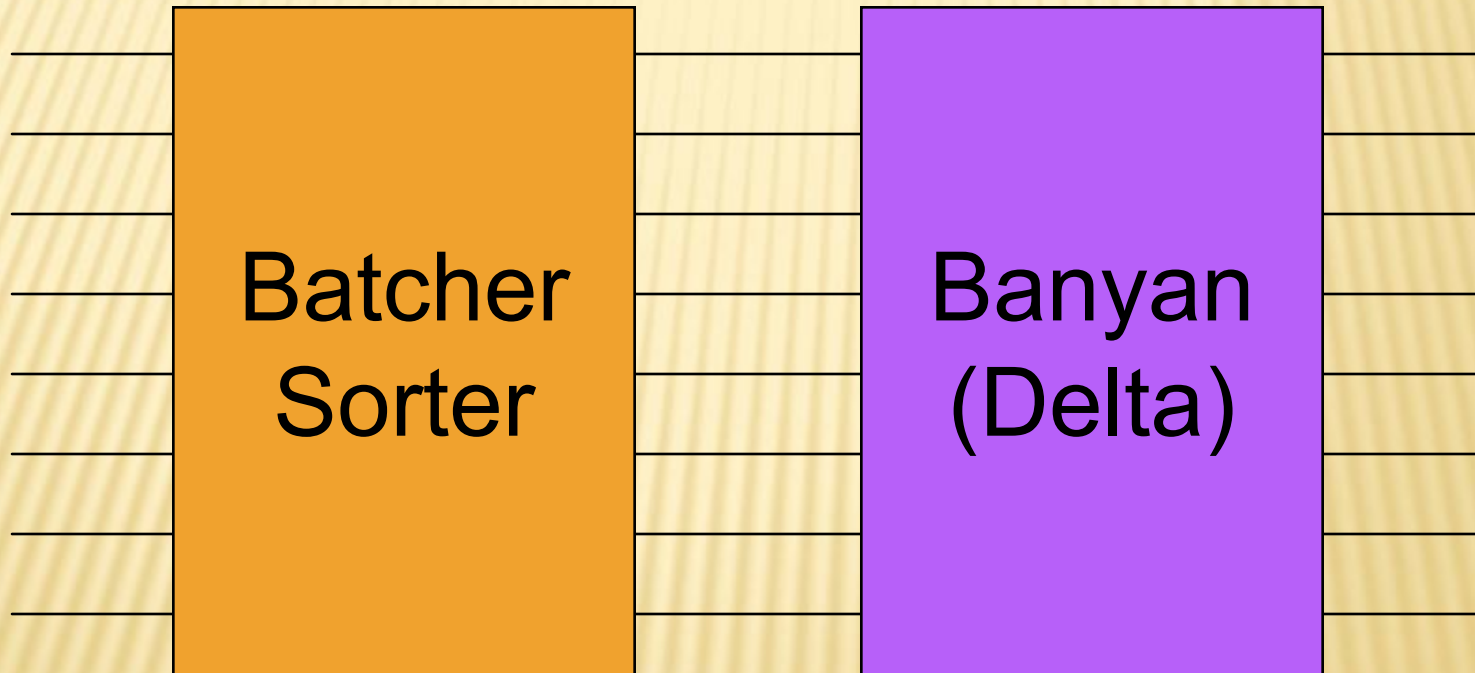
PERFORMANCE DEGRADATION



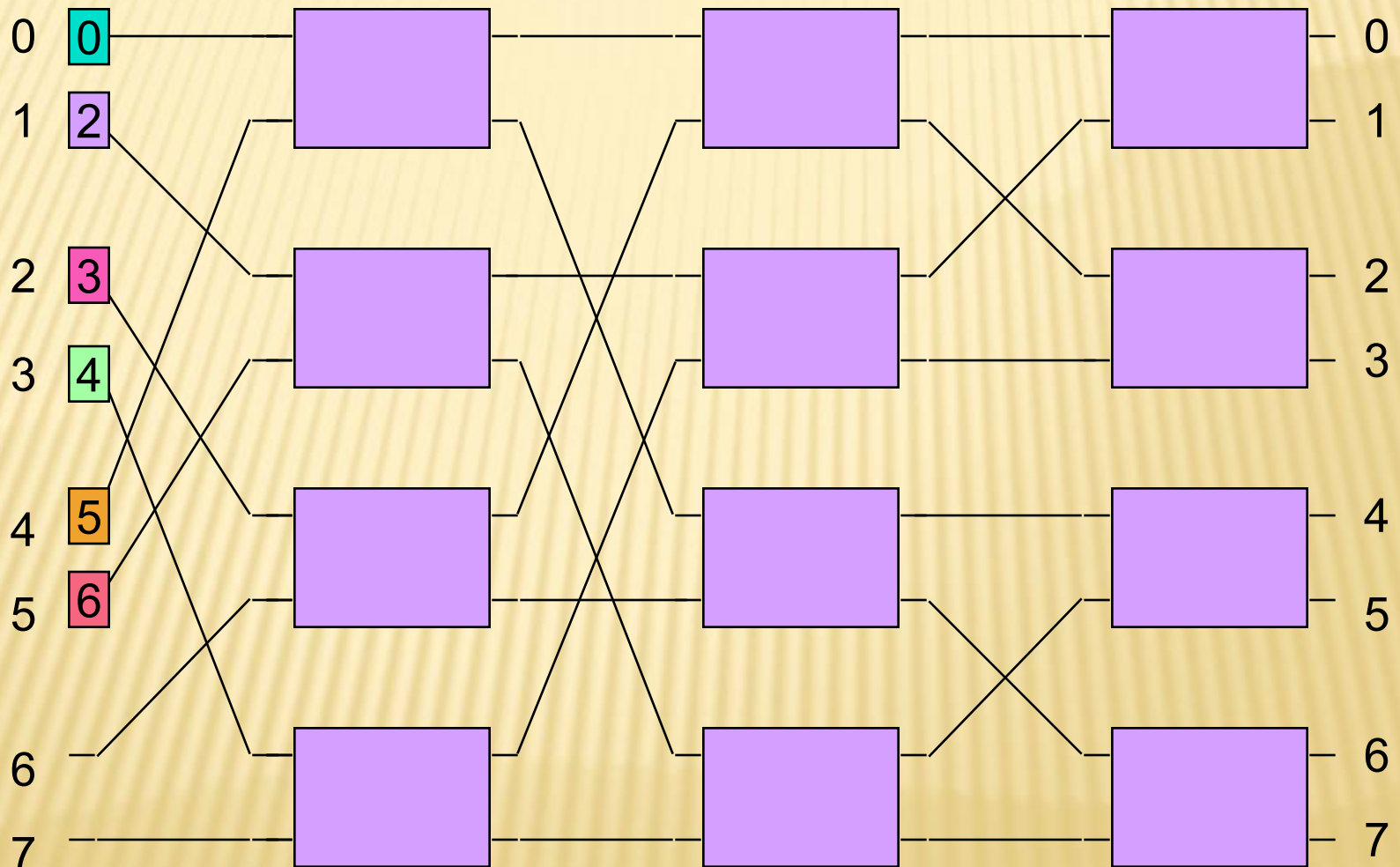
A SOLUTION: BATCHER SORTER

- One solution to the contention problem is to sort the cells into monotonically increasing order based on desired destination port
- Done using a bitonic sorter called a Batcher
- Places the M cells into gap-free increasing sequence on the first M input ports
- Eliminates duplicate destinations

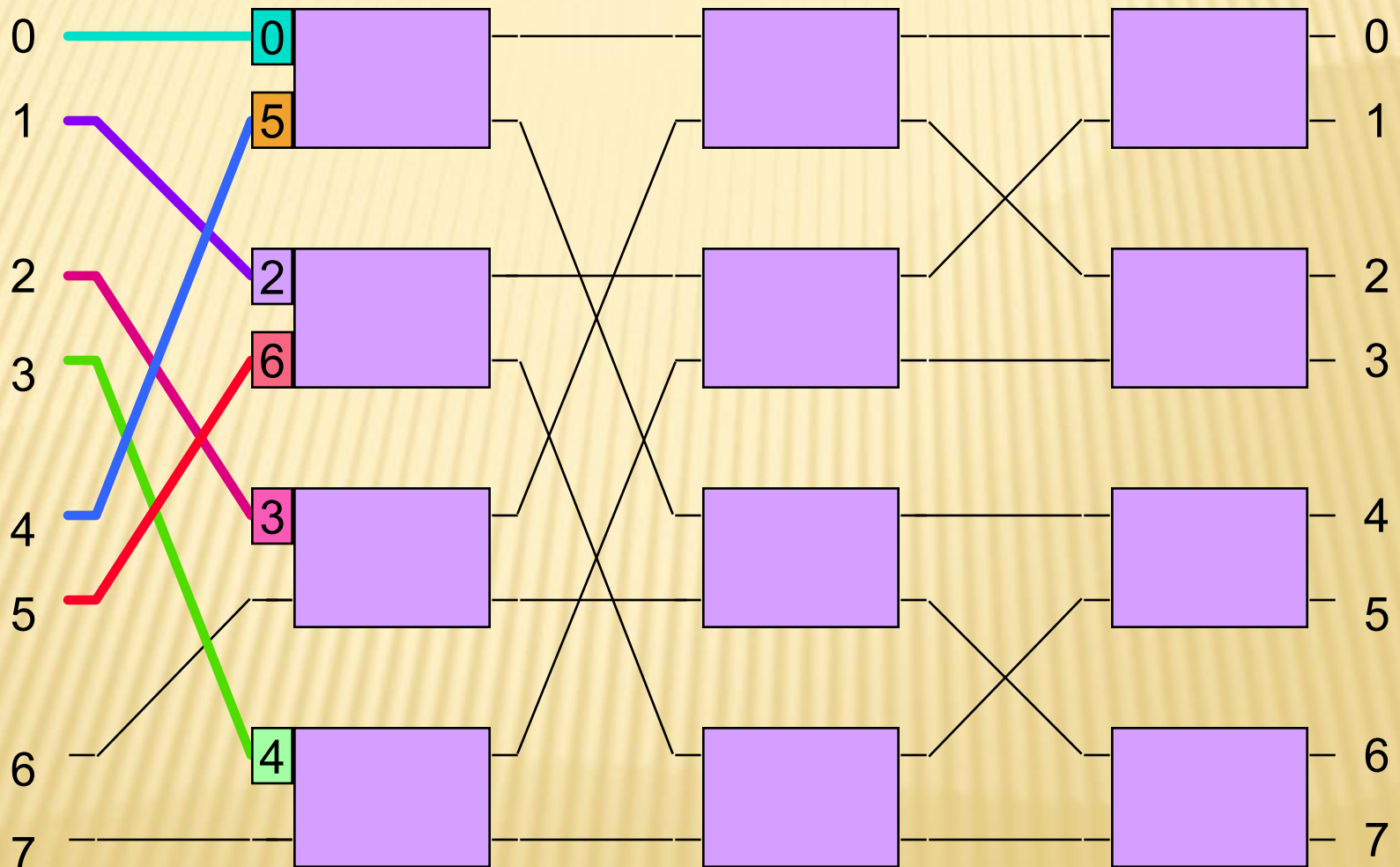
BATCHER-BANYAN



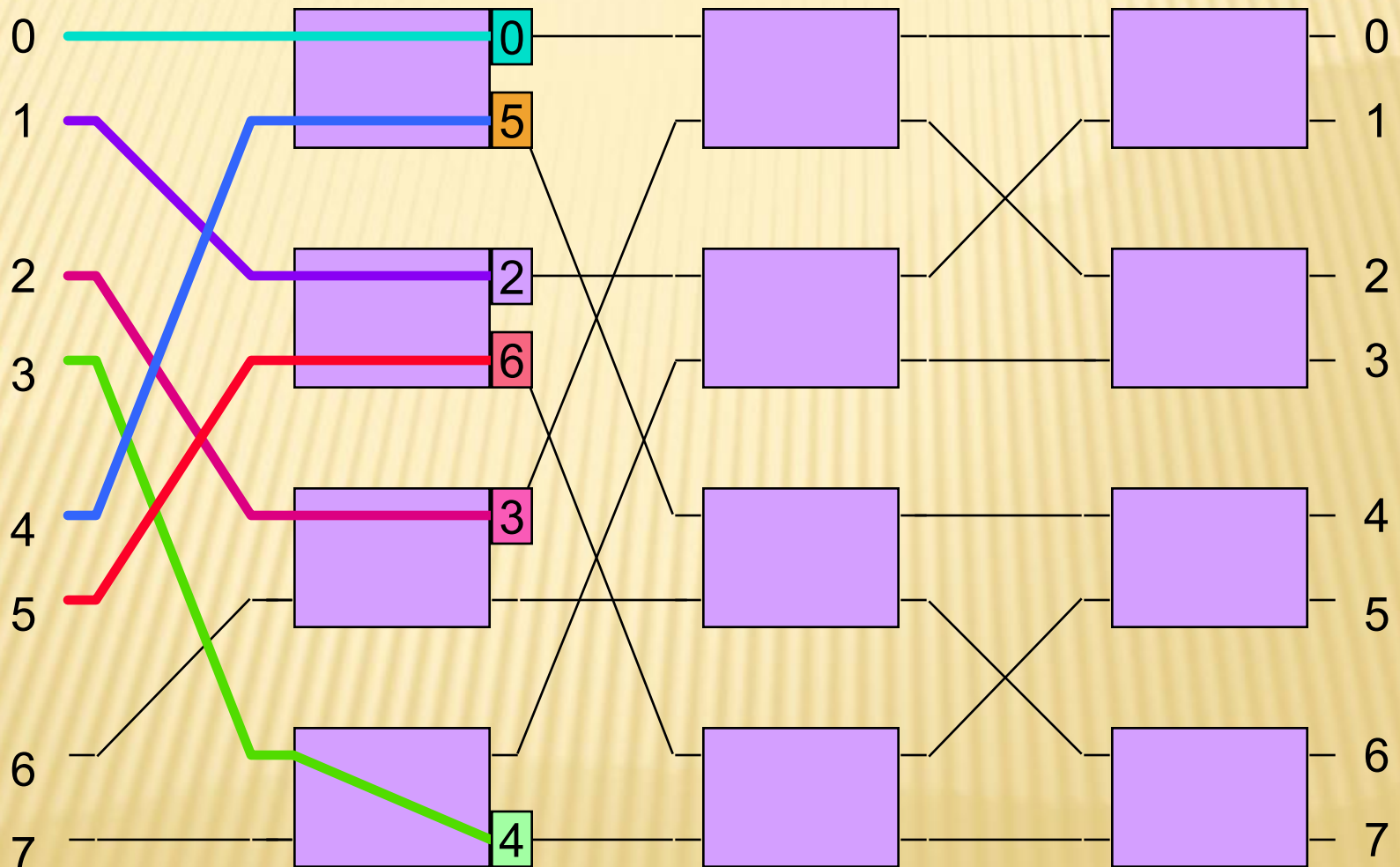
BATCHER-BANYAN EXAMPLE



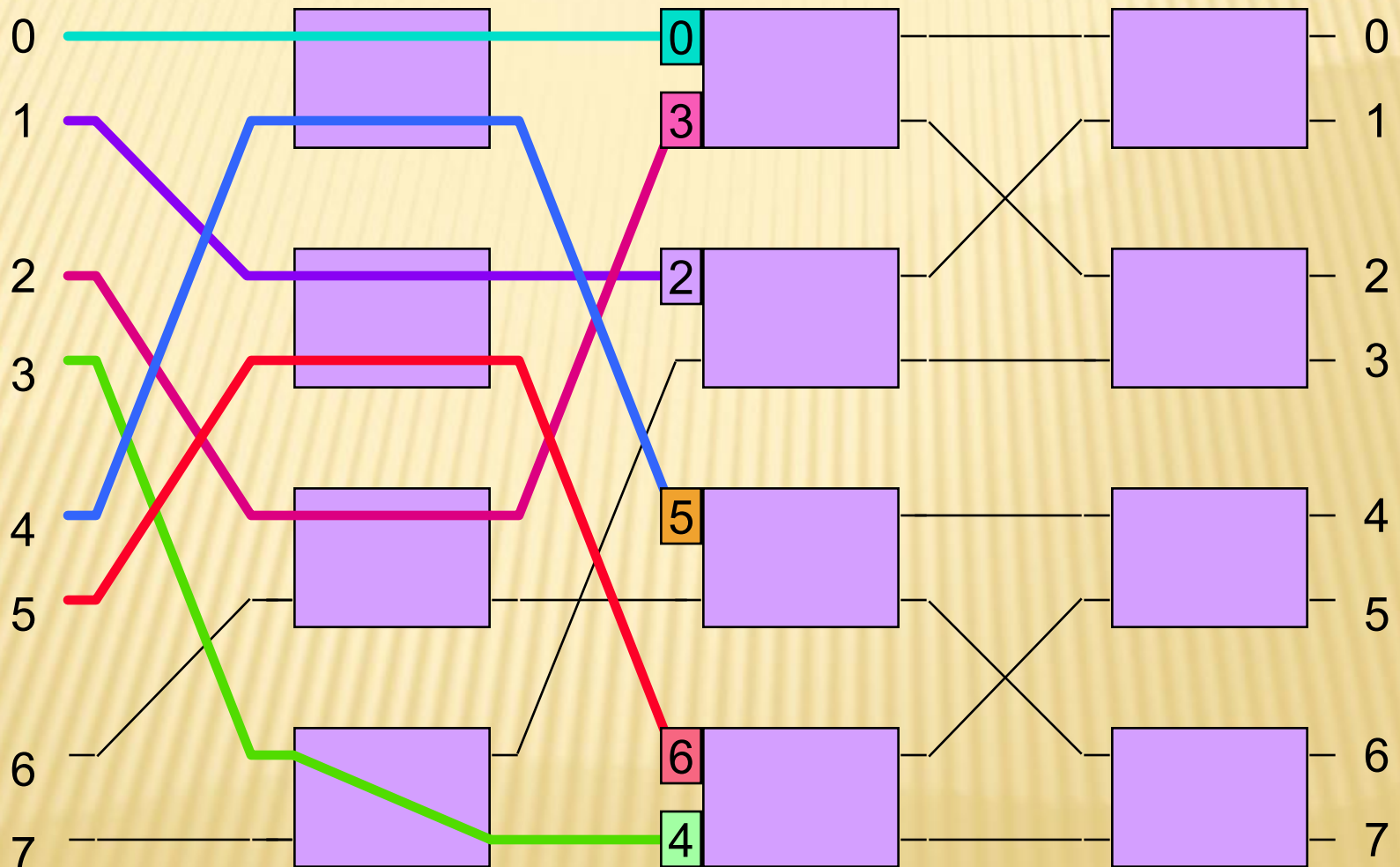
BATCHER-BANYAN EXAMPLE



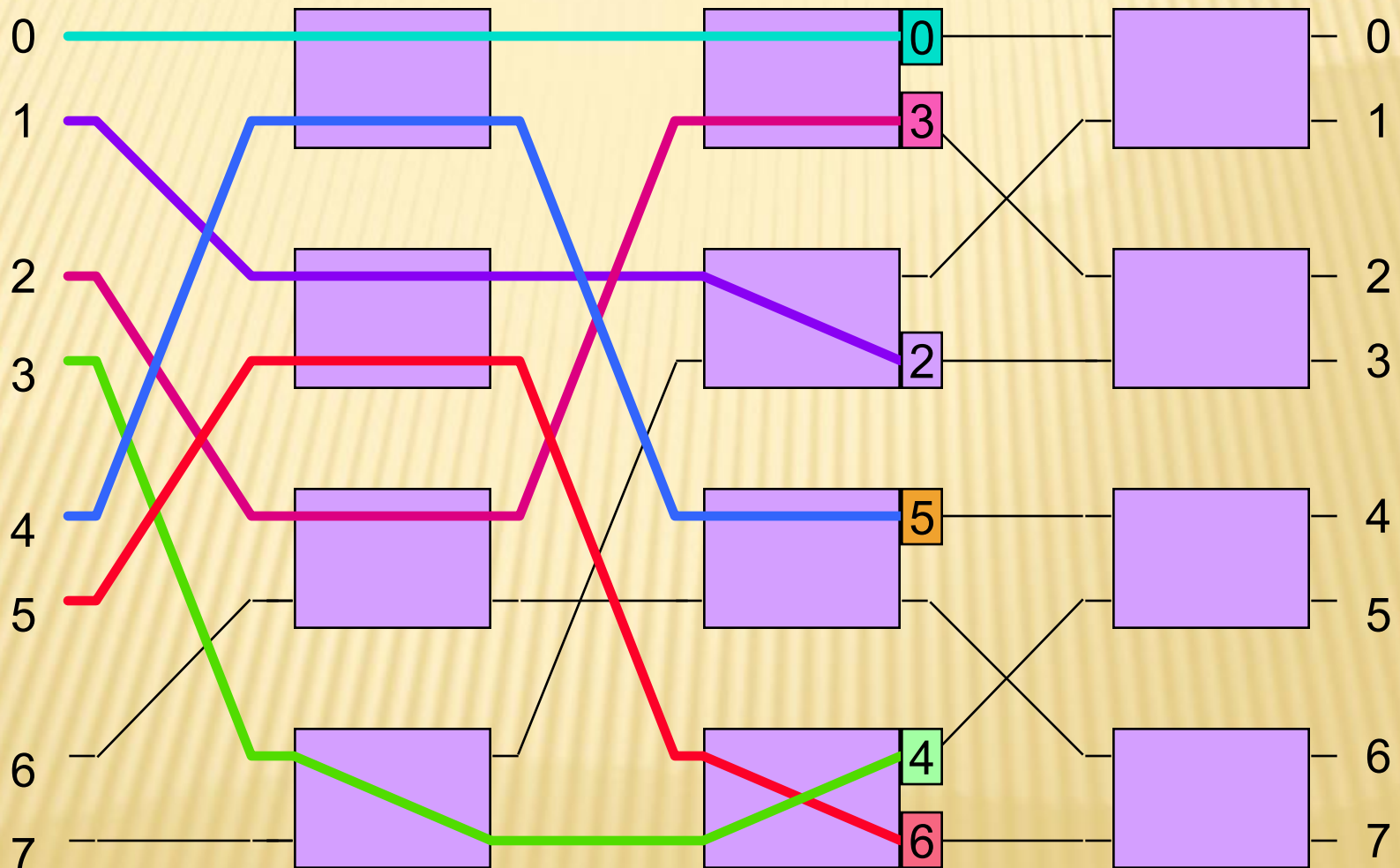
BATCHER-BANYAN EXAMPLE



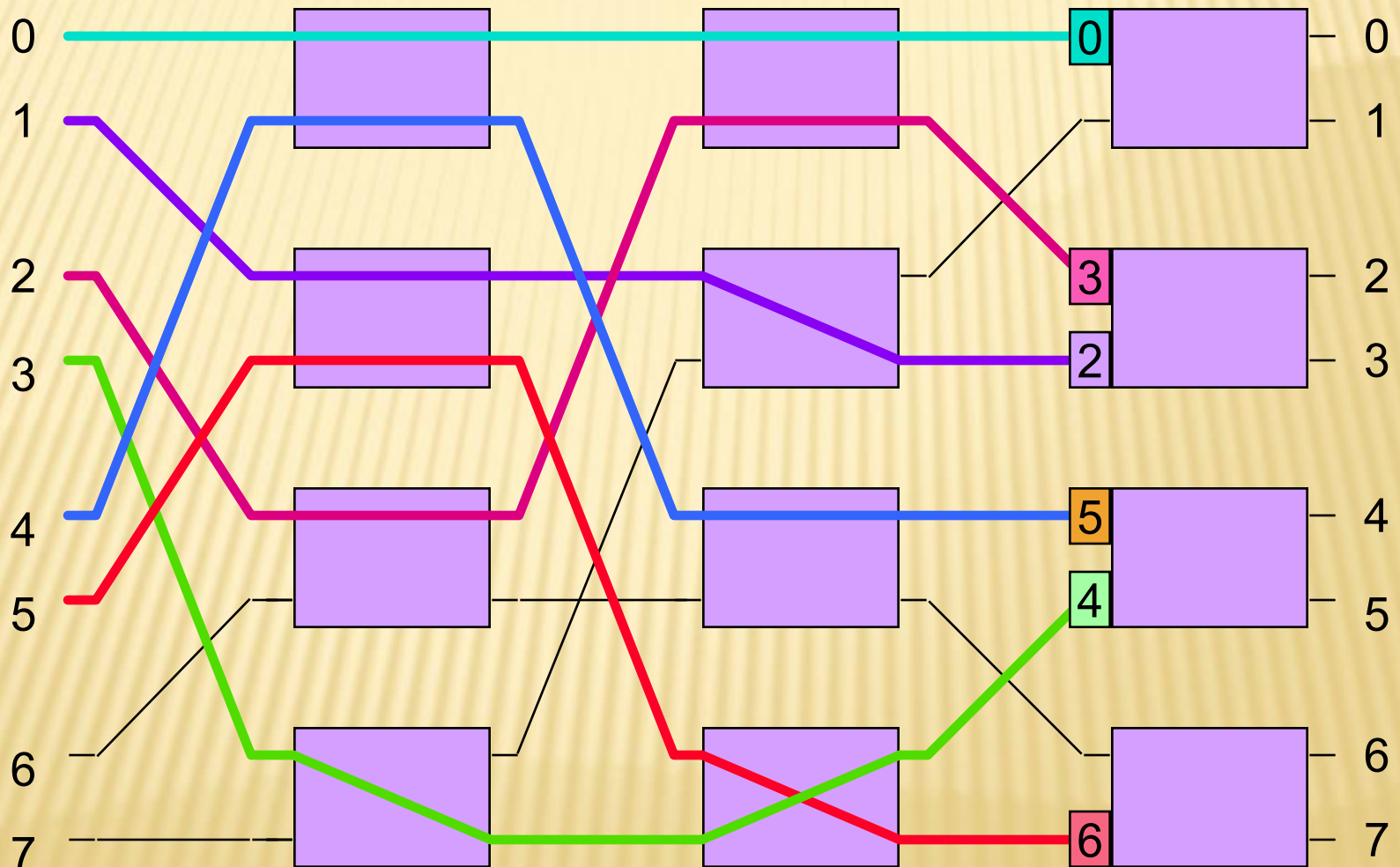
BATCHER-BANYAN EXAMPLE



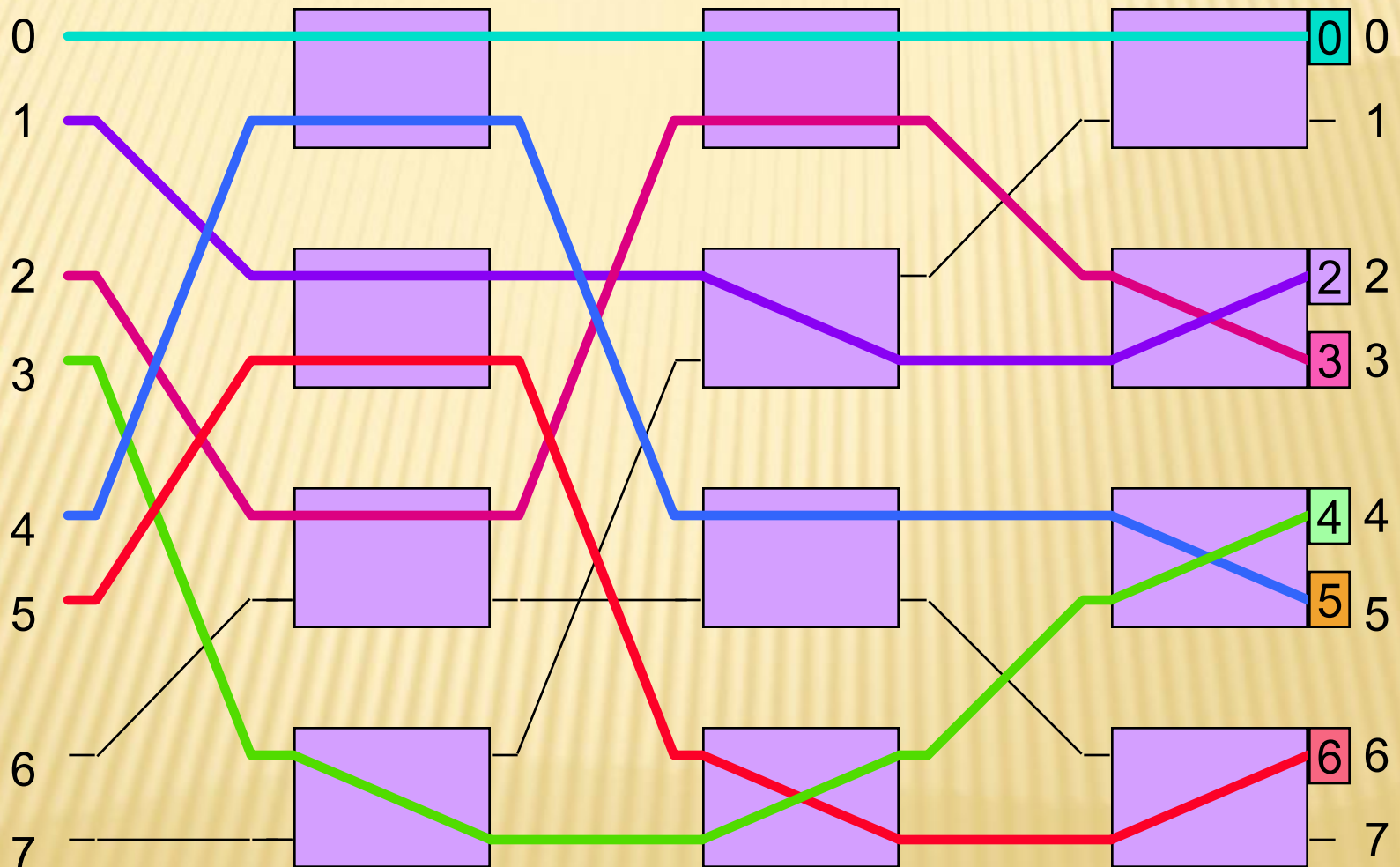
BATCHER-BANYAN EXAMPLE



BATCHER-BANYAN EXAMPLE



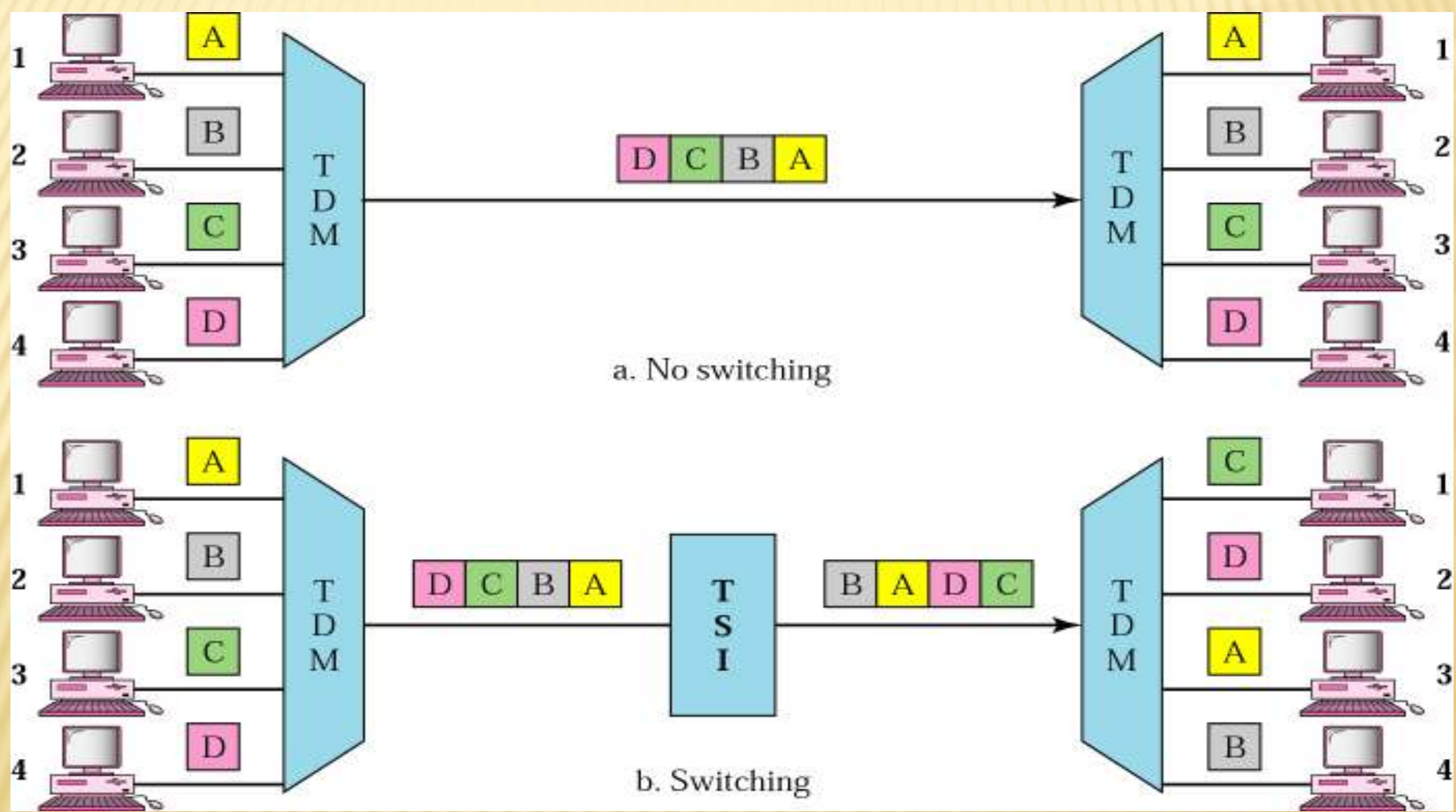
BATCHER-BANYAN EXAMPLE



TIME DIVISION SWITCHING

- ❖ **Time-division switching** : uses time-division multiplexing to achieve switching.
- ❖ **Two methods used are:**
 - Time-slot interchange (TSI) changes the order of the slots based on the desired connection.
 - Time Division Multiplexing (TDM) bus

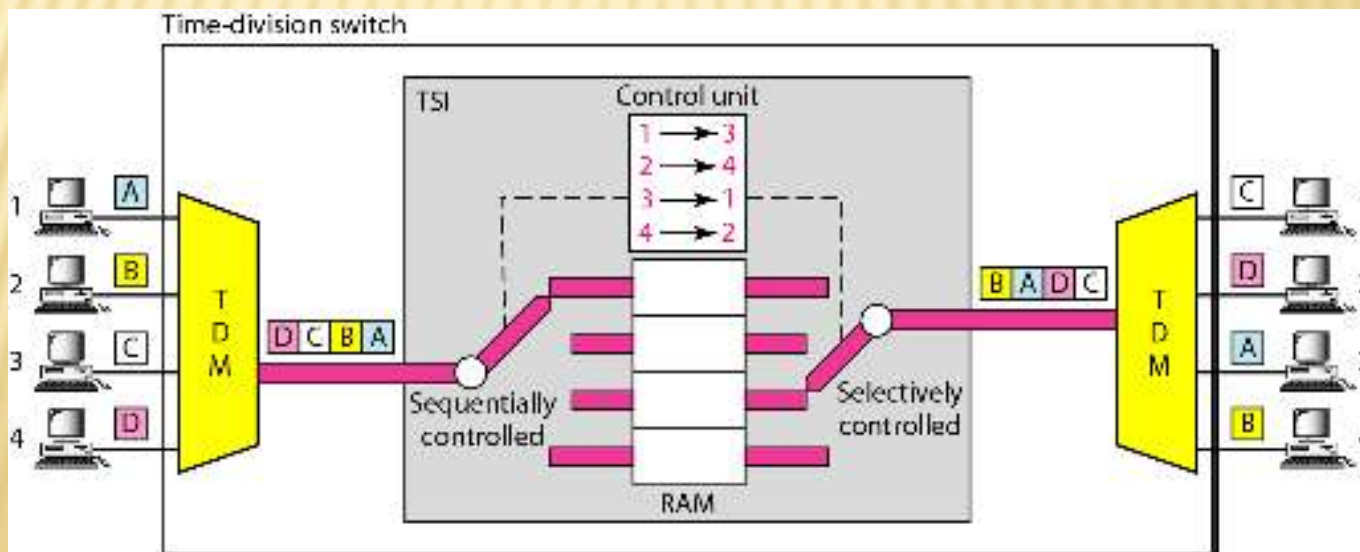
TIME-DIVISION MULTIPLEXING, WITHOUT AND WITH A TIME-SLOT INTERCHANGE



TDM : Time-division Multiplexing
TSI : Time-Slot Interchange

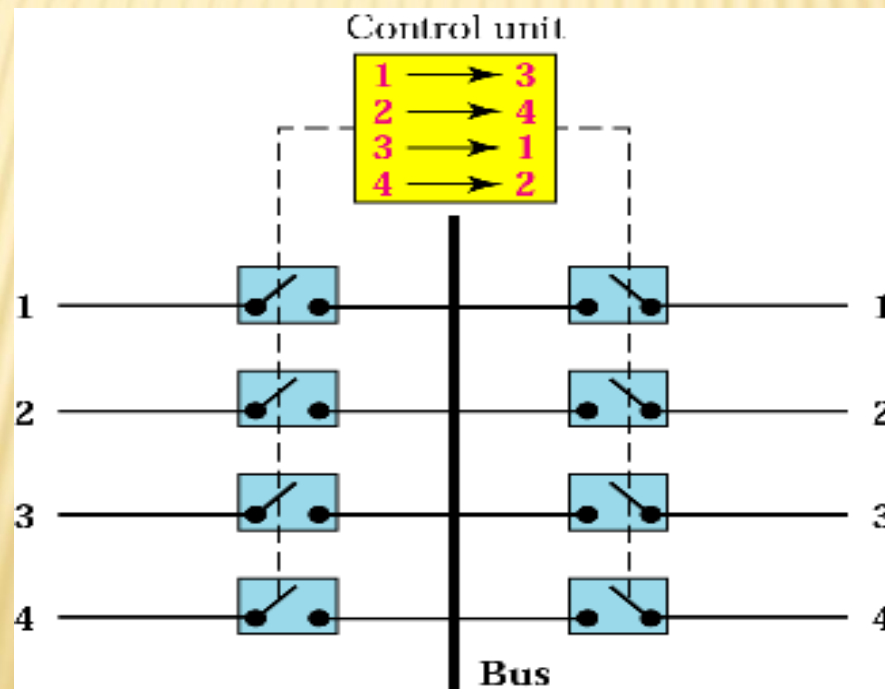
TIME-SLOT INTERCHANGE

- ❑ TSI consists of random access memory (RAM) with several memory locations. The size of each location is the same as the size of a single time slot.
- ❑ The number of locations is the same as the number of inputs.
- ❑ The RAM fills up with incoming data from time slots in the order received. Slots are then sent out in an order based on the decisions of a control unit.



TDM BUS

- Input and output lines are connected to a high-speed bus through input and output gates (microswitches)
- Each input gate is closed during one of the four slots.
- During the same time slot, only one output gate is also closed. This pair of gates allows a burst of data to be transferred from one specific input line to one specific output line using the bus.
- The control unit opens and closes the gates according to switching need.



COMPARISON OF SDM AND TDM

➤ SDM

❑ Advantage:

- ❖ Instantaneous.

❑ Disadvantage:

- ❖ Number of cross points required.

➤ TDM

❑ Advantage:

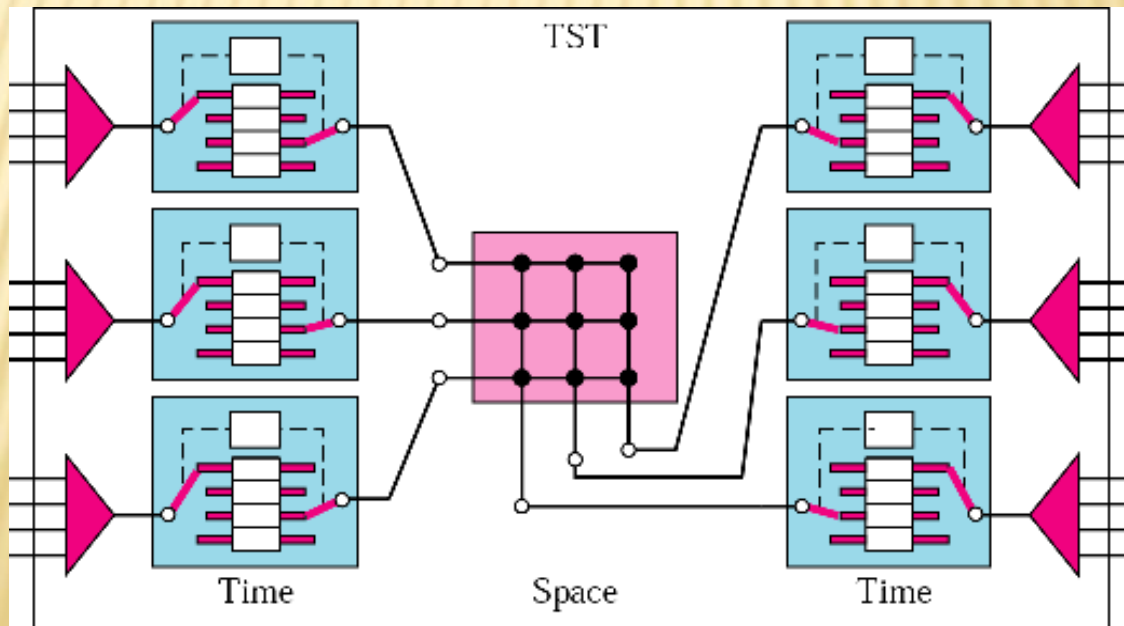
- ❖ No cross points.

❑ Disadvantage:

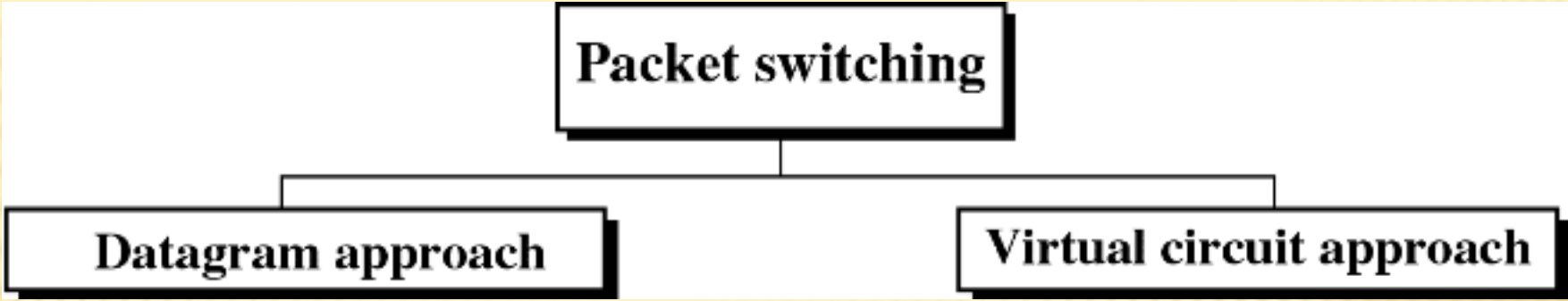
- ❖ Processing delay.

TST SWITCH

- ✗ Combine Space division and time division switching.
- ✗ This results in switches that are optimized both physically (the number of crosspoints) and temporally (the amount of delay).
- ✗ Various types are: time-space-time (TST), time-space-space-time (TSST), space-time-time-space (STTS), etc.



Packet switching



```
graph TD; A[Packet switching] --> B[Datagram approach]; A --> C[Virtual circuit approach];
```

Datagram approach

Virtual circuit approach

TWO MAJOR PACKET SWITCHING MODES :

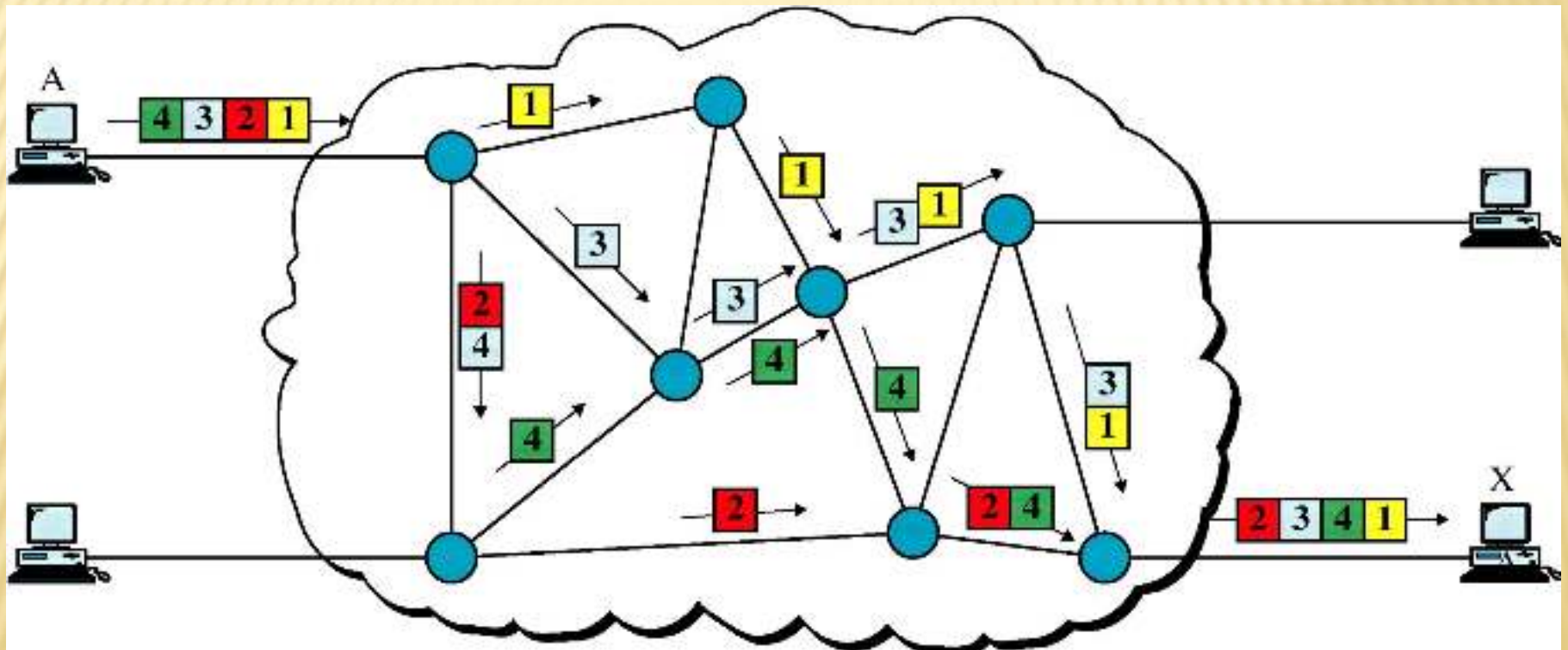
(1) connectionless packet switching, also known as datagram switching:

Each packet includes complete addressing or routing information. The packets are routed individually, sometimes resulting in different paths and out-of-order delivery.

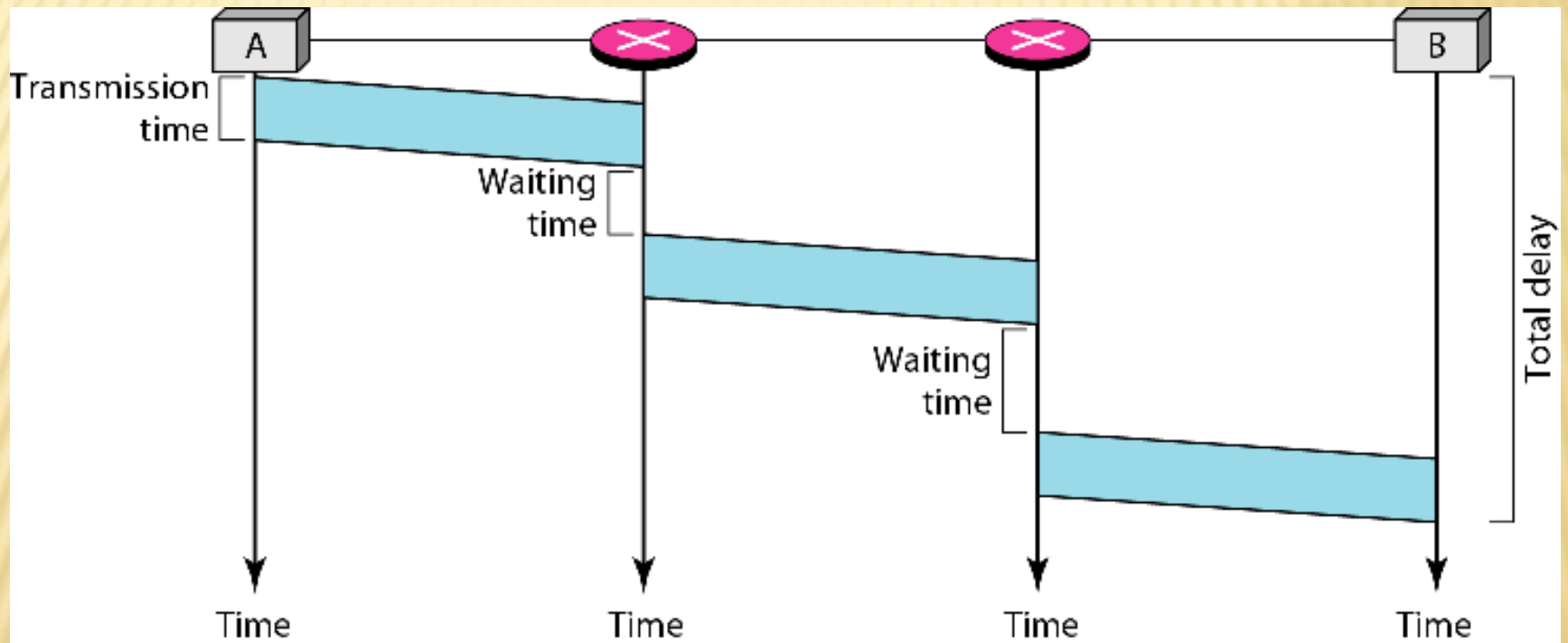
(2) connection-oriented packet switching, also known as virtual circuit switching

A connection is defined and pre allocated in each involved node during a connection phase before any packet is transferred. The packets include a connection identifier rather than address information, and are delivered in order.

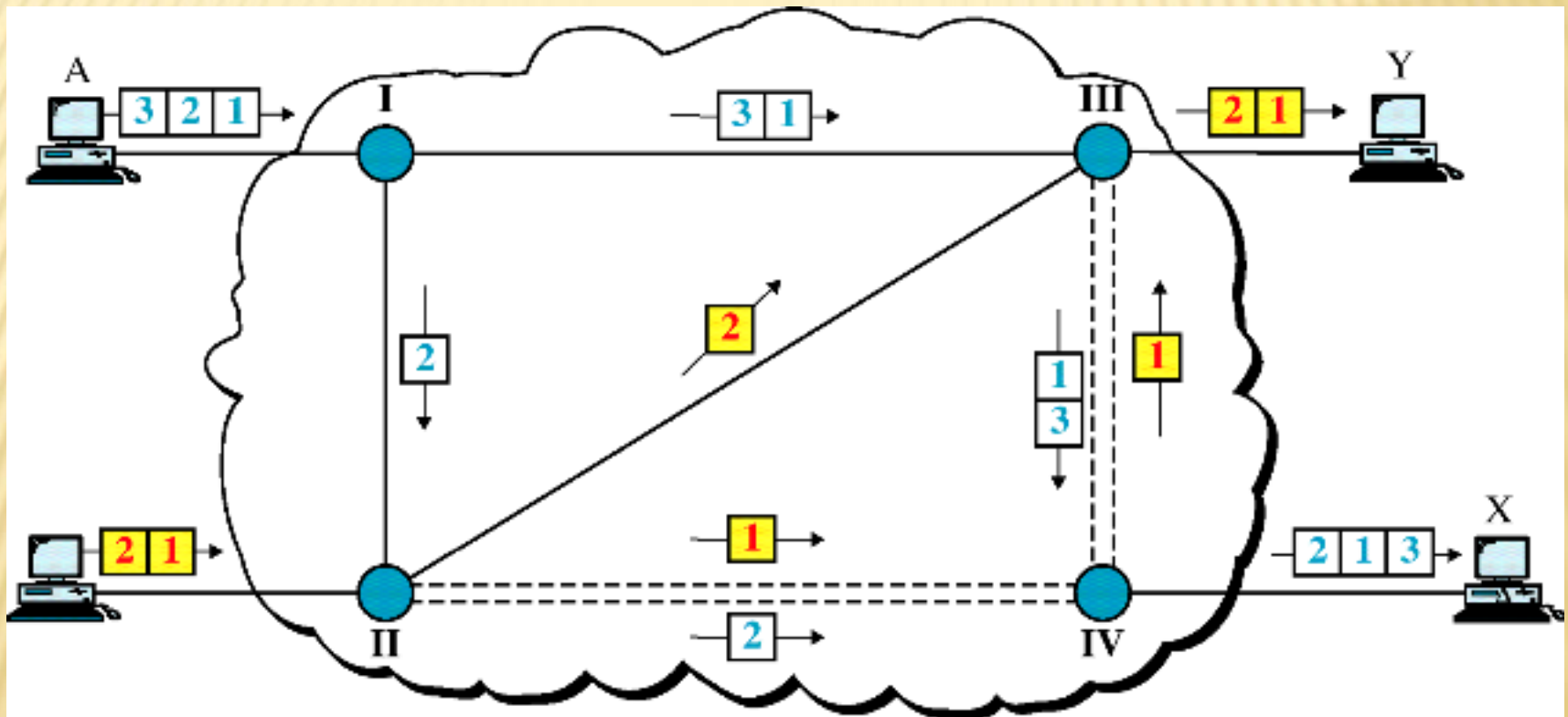
Datagram Approach



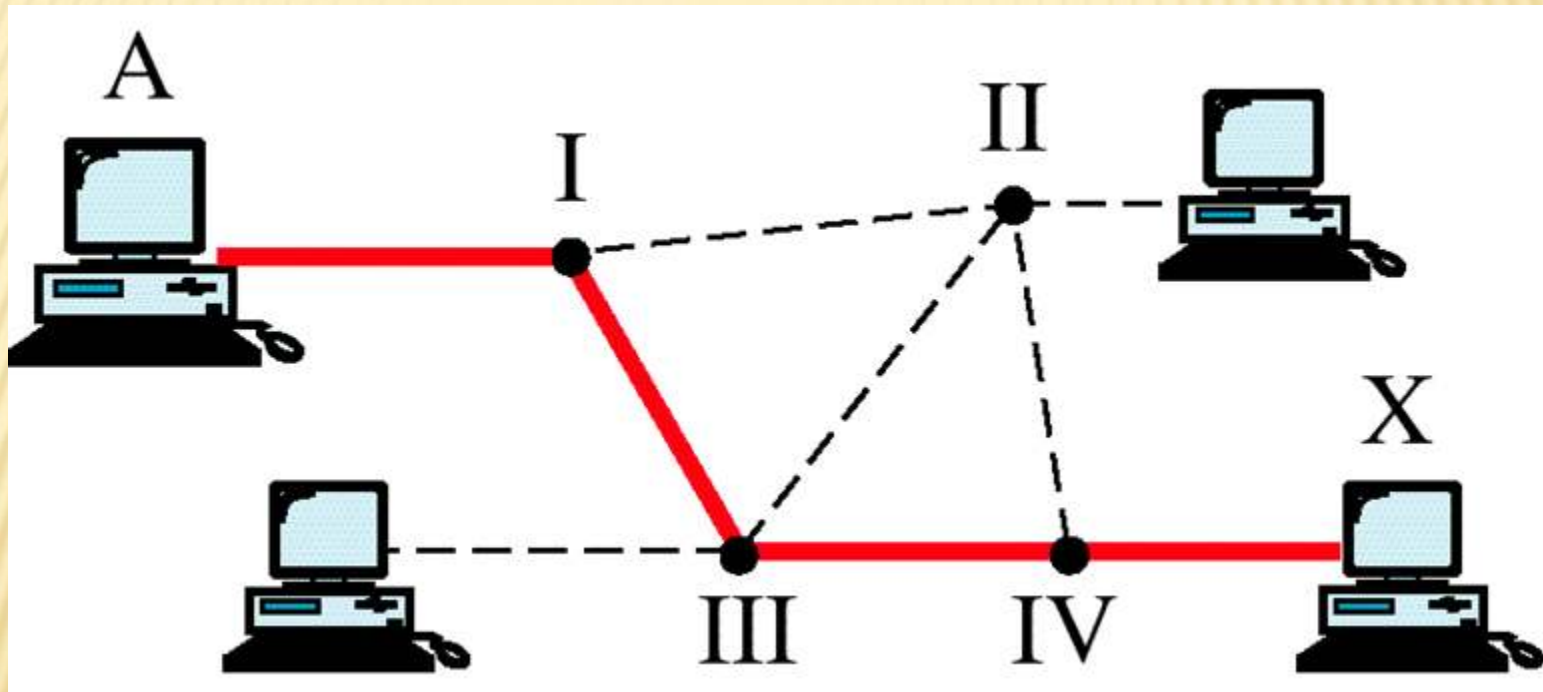
Delay in a datagram network



Datagram Approach and Multiple Channels

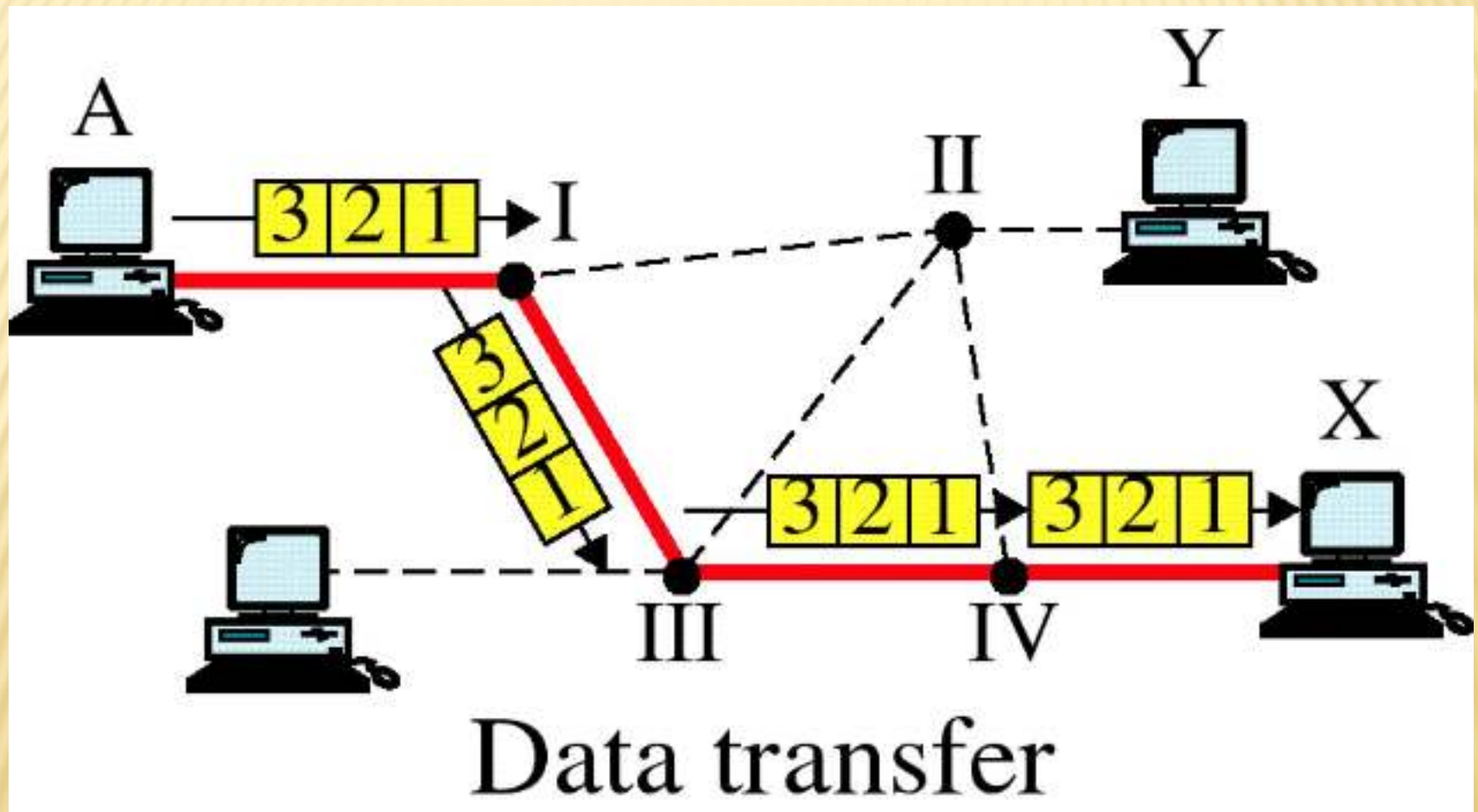


Switched Virtual Circuit

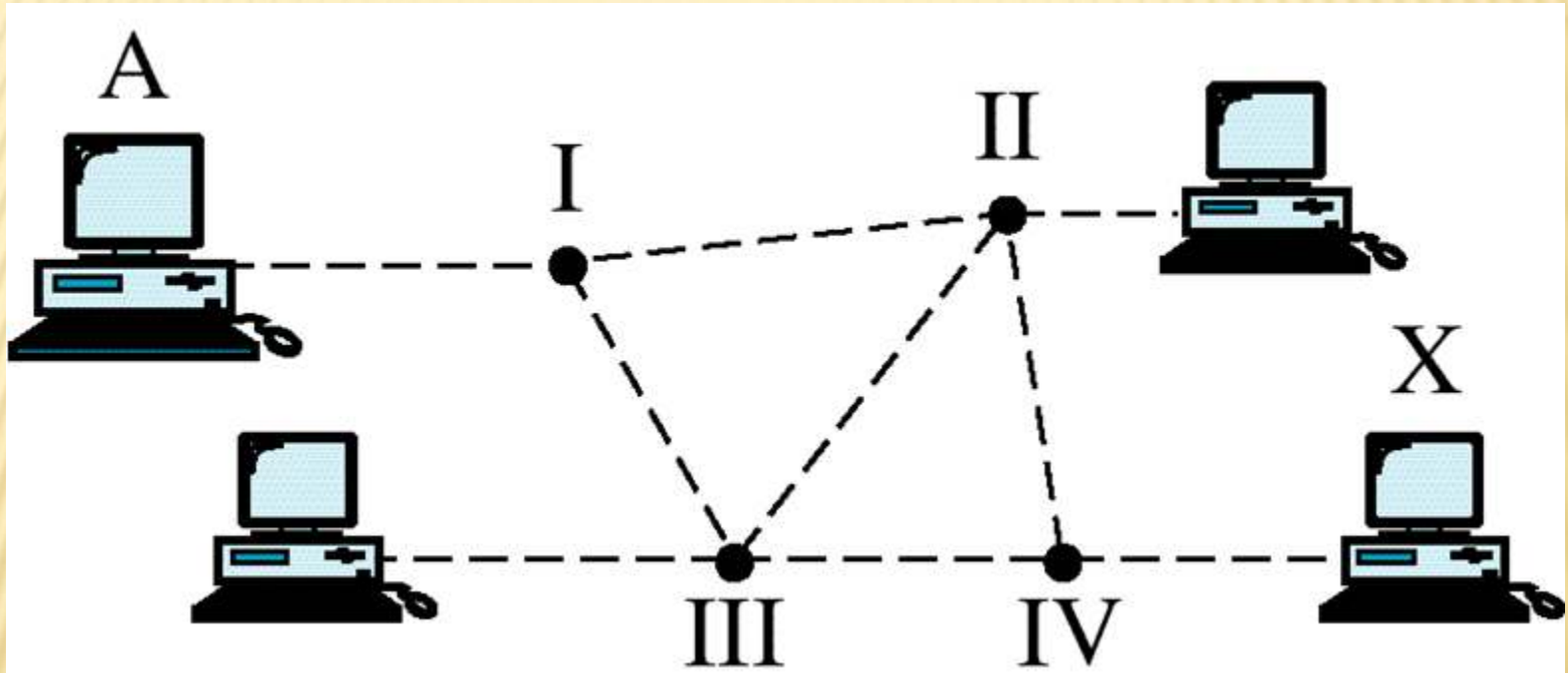


Connection Establishment

Switched Virtual Circuit

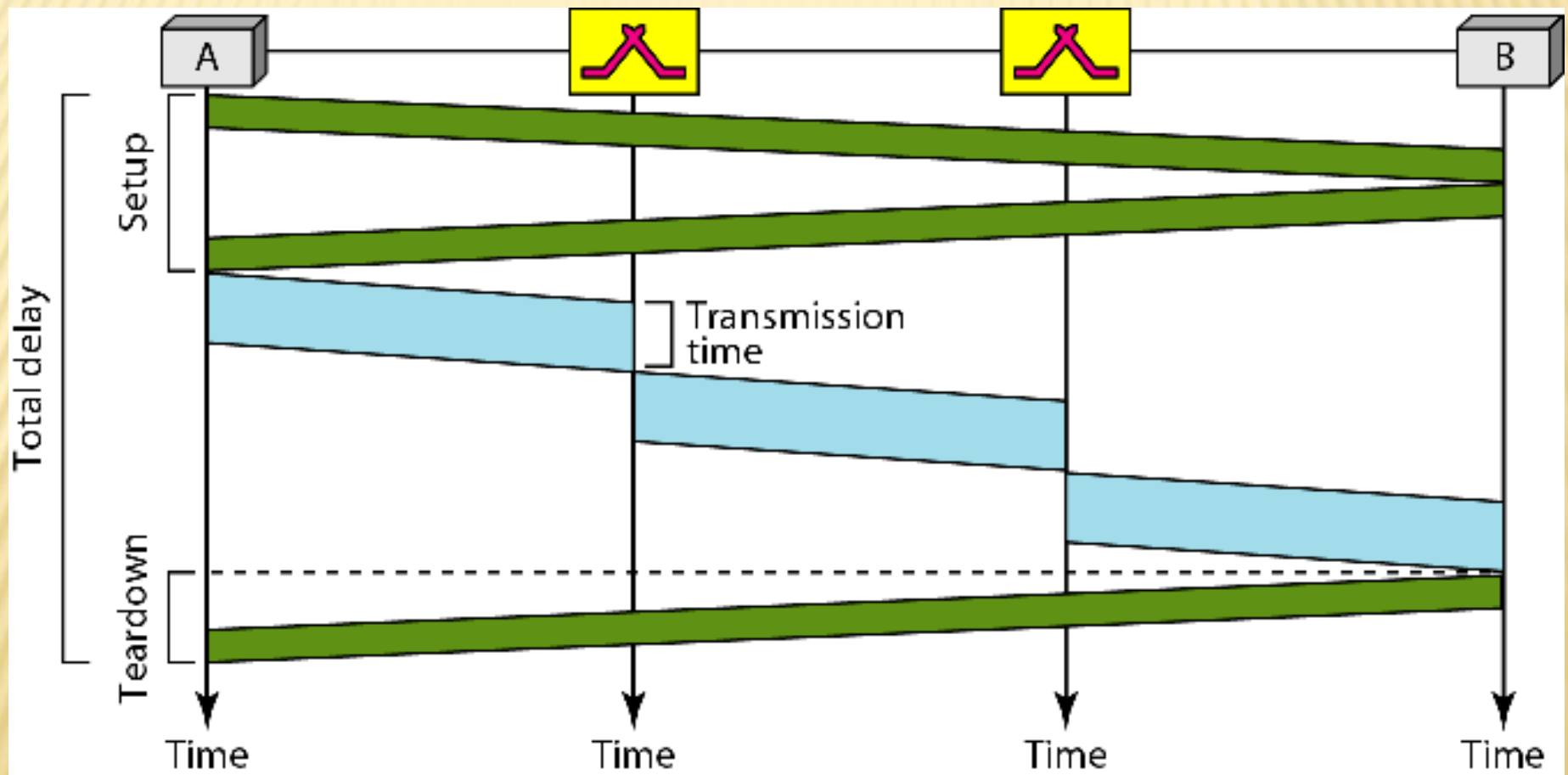


Switched Virtual Circuit

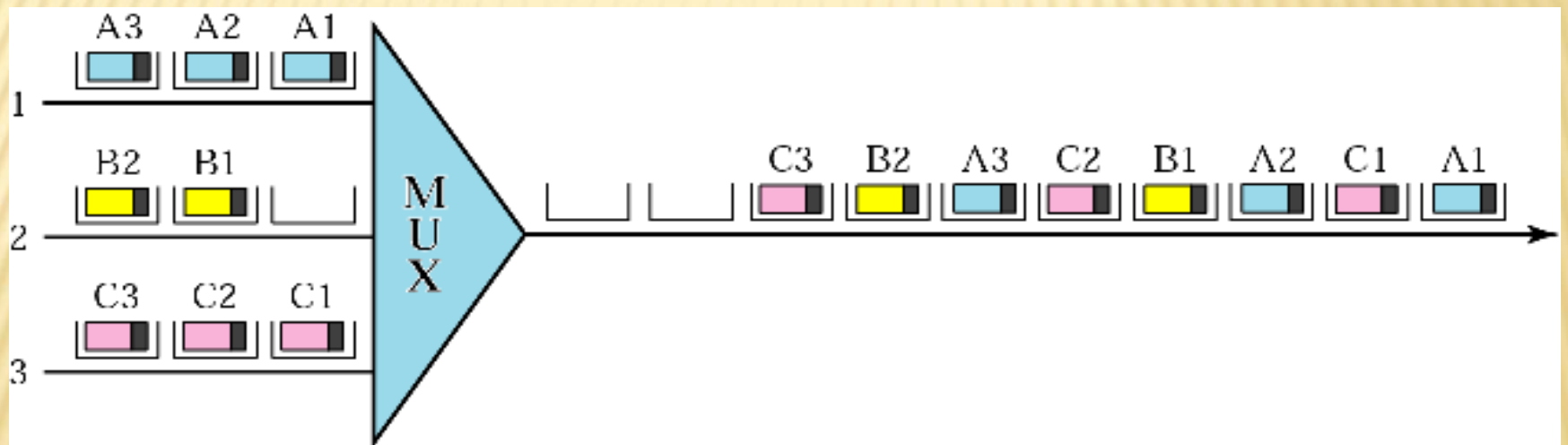


Connection release

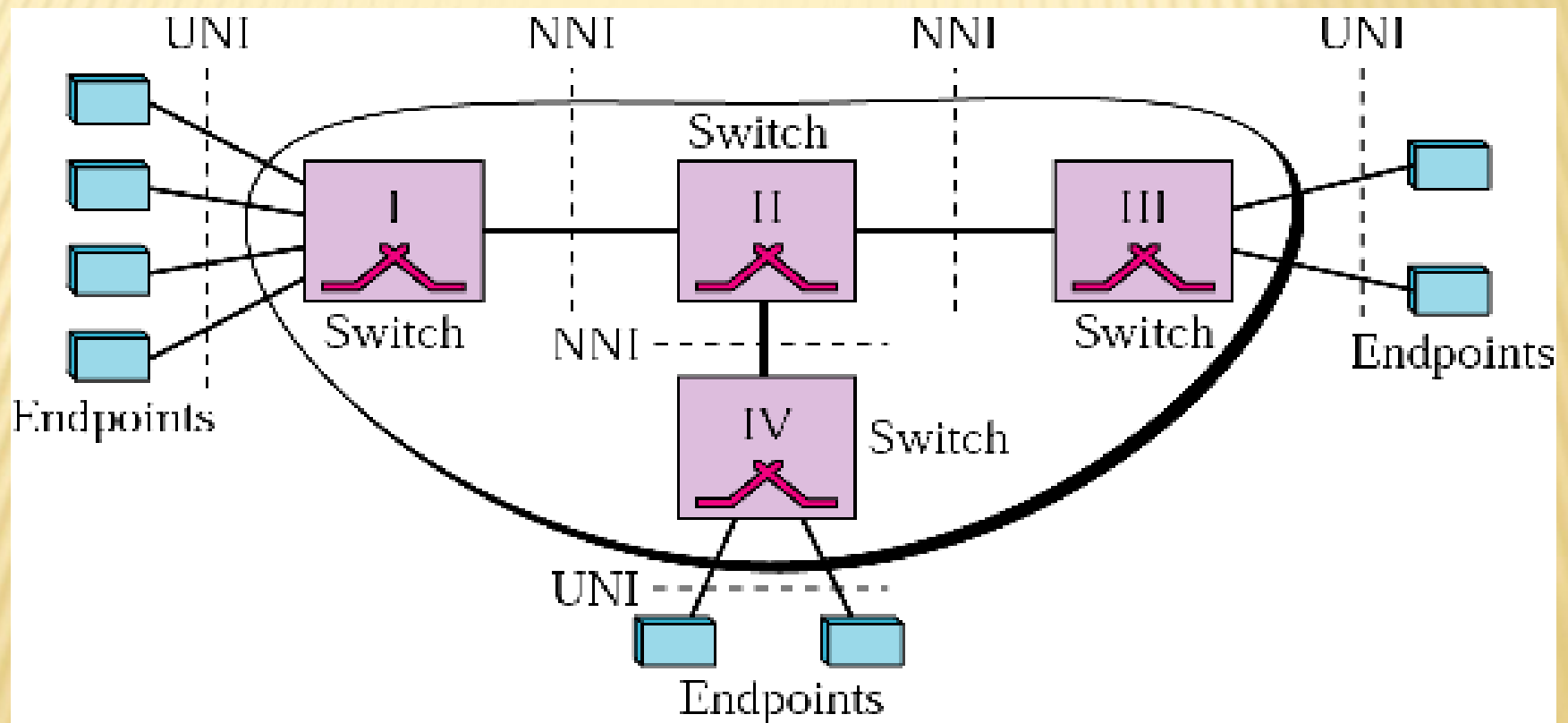
Delay in a virtual-circuit network



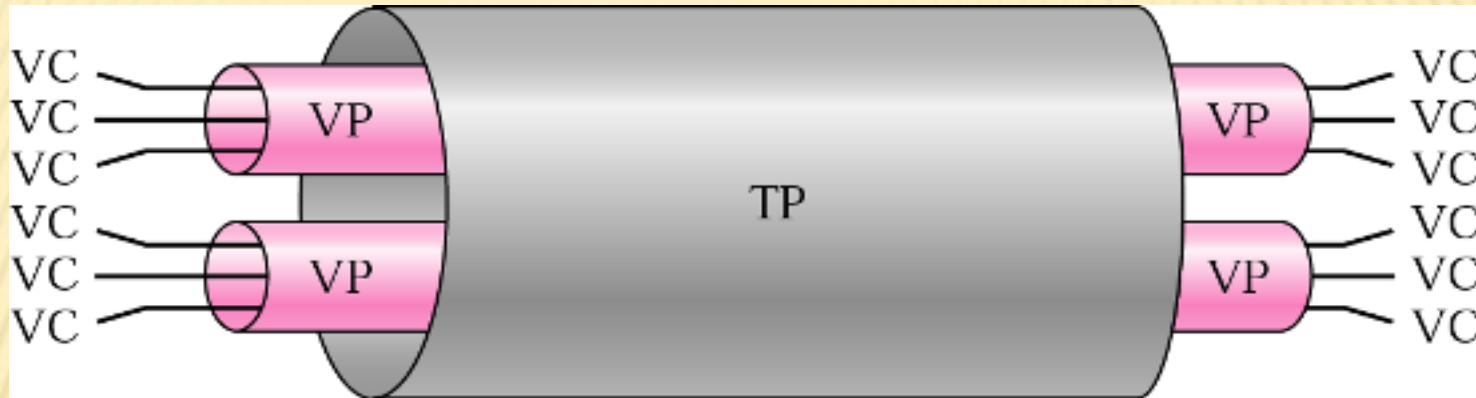
ATM multiplexing



Architecture of an ATM network



Terminal Path, Virtual Paths, and Virtual Circuits

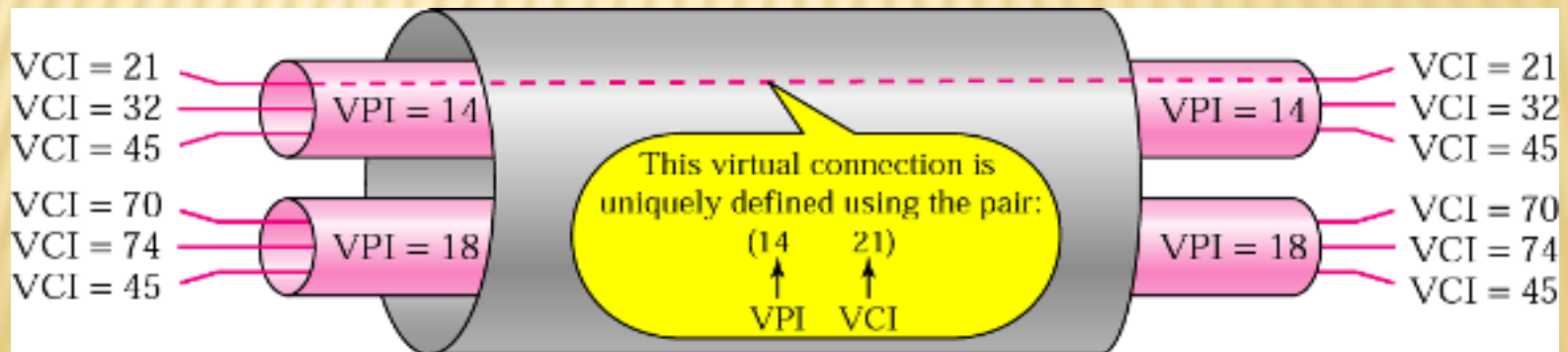


TP Terminal Path

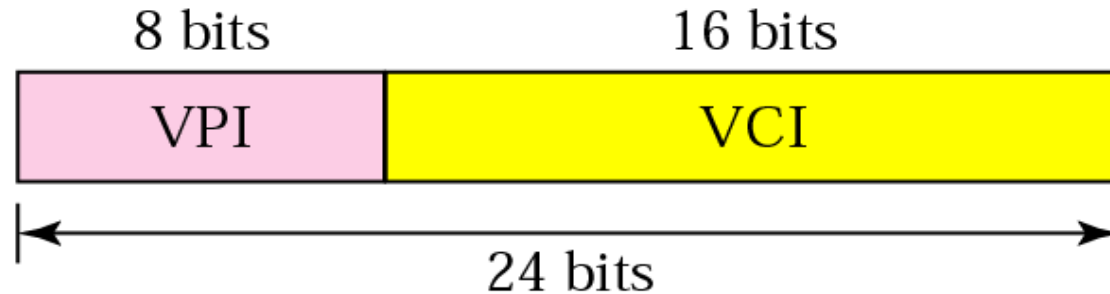
VP Virtual Path

VC Virtual Circuit

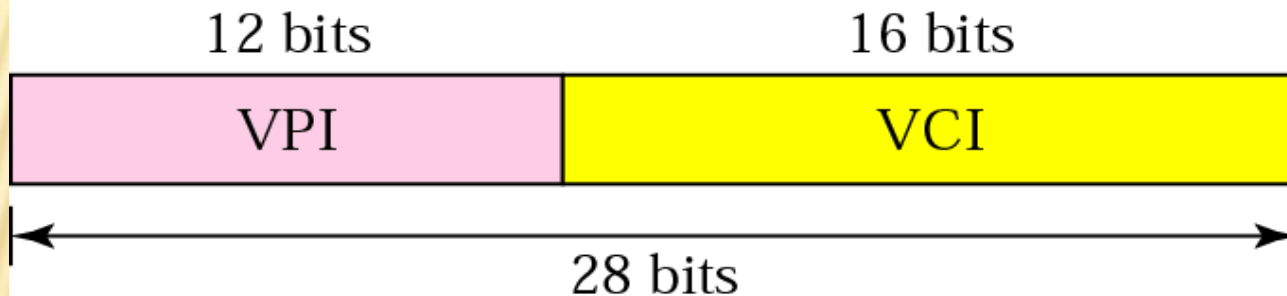
A virtual connection is defined by a pair of numbers: VPI and VCI



Virtual connection identifiers in UNIs and NNIs



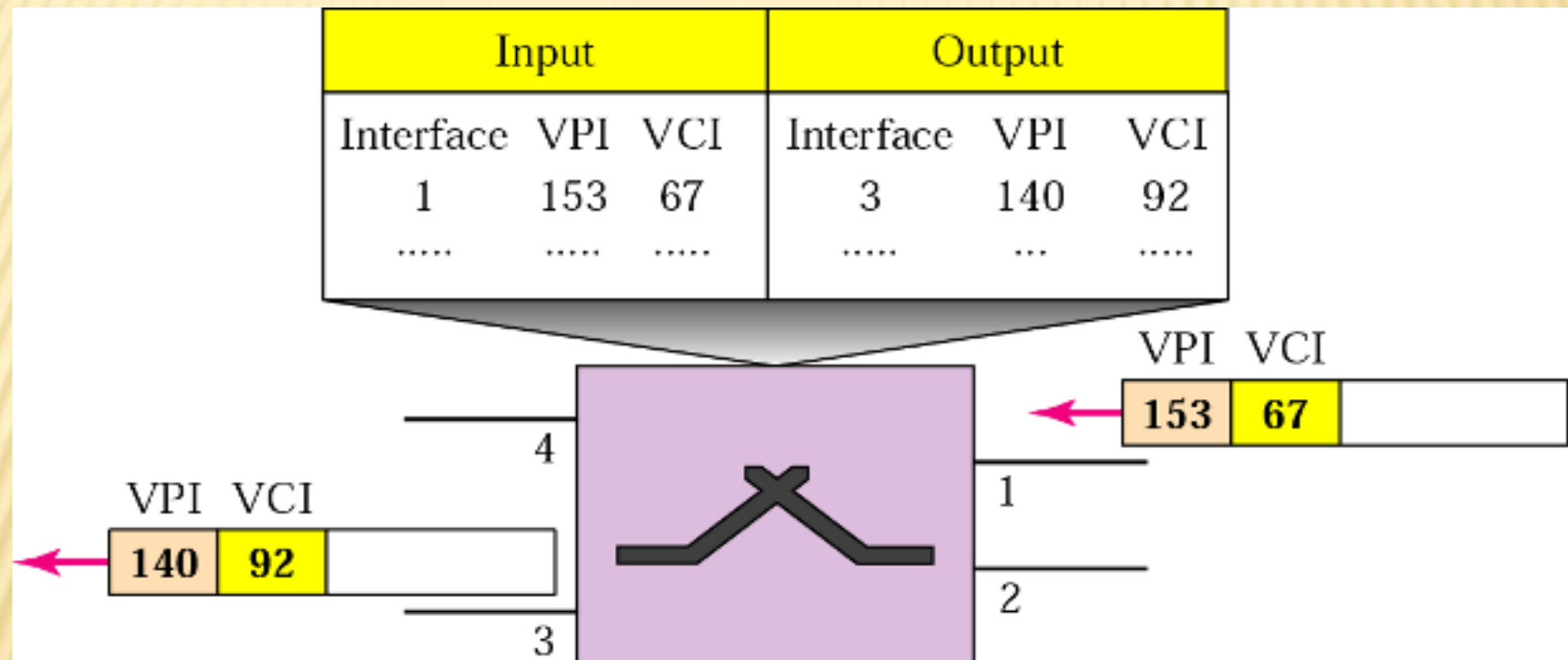
a. VPI and VCI in a UNI



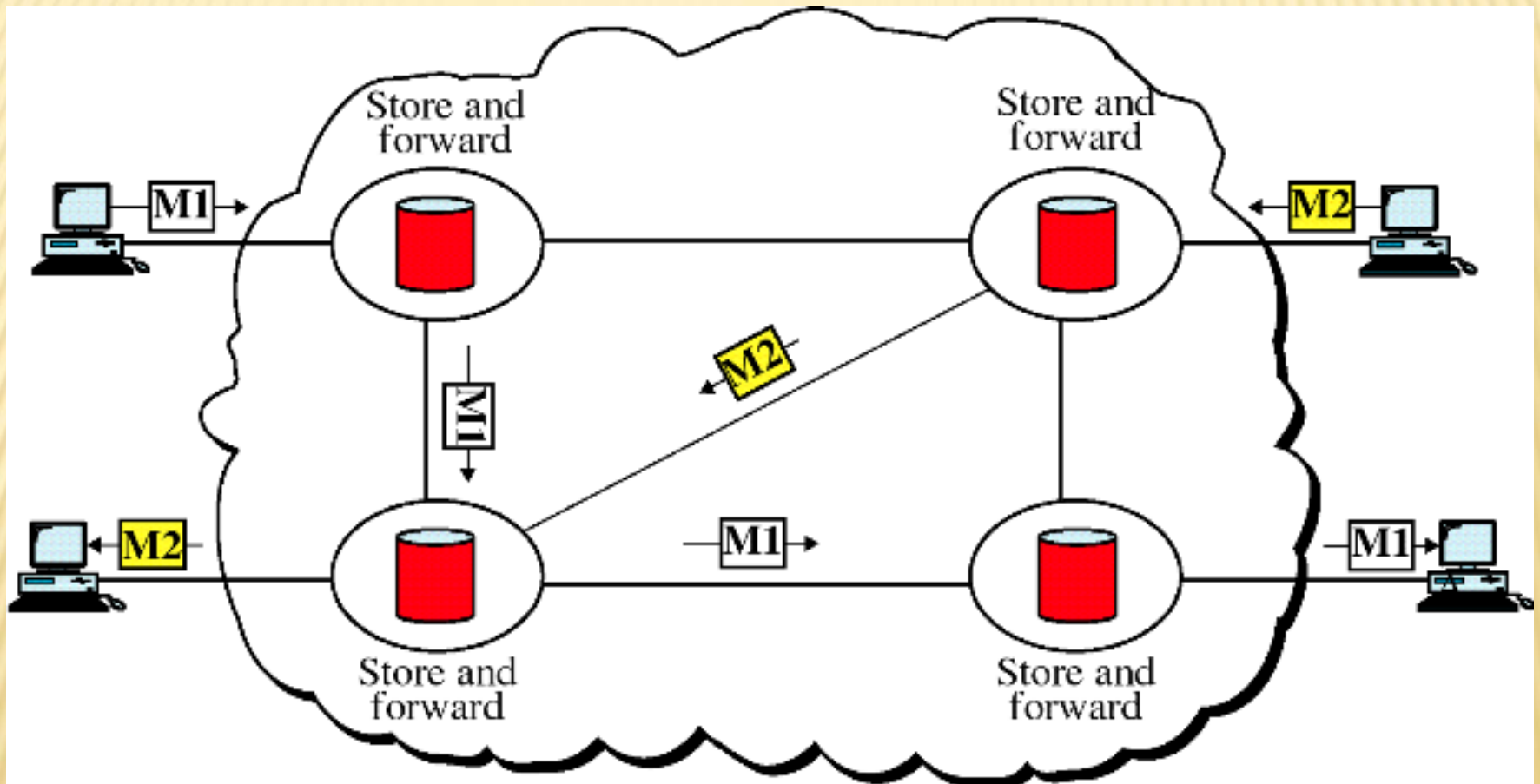
b. VPI and VCI in an NNI

UNI User-Network Interface
NNI Network-Network Interface

Routing with a switch



Message Switching



Each message is treated as a separate entity and contains addressing information, and at each switch this information is read and the transfer path to the next switch is decided.

ATM SWITCHING

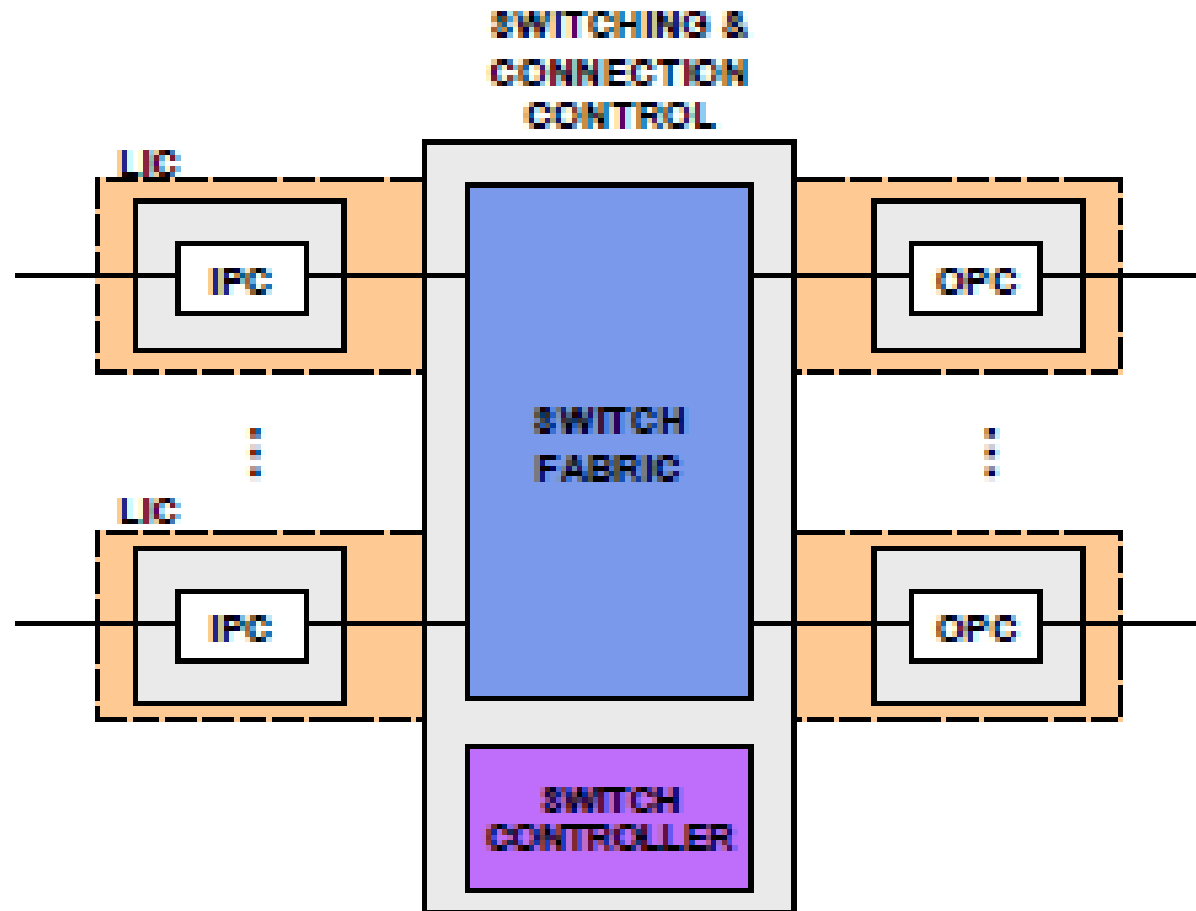
- ATM is a connection-oriented transport concept
 - An end-to-end connection (virtual channel) established prior to transfer of cells
 - Signaling used for connection set up and release
 - Data transferred in fixed 53 octets long cells (5 octets for header and 48 octets for payload)
- Cells routed based on two header fields
 - virtual path identifier (VPI) - 8 bits for UNI and 12 bits for NNI
 - virtual channel identifier (VCI) - 16 bits for UNI and NNI
 - combination of VPI and VCI determines a specific virtual connection between two end-points
- When an ATM cell arrives to an ATM switch, VPI/VCI in the 5-octet cell header is used to point to a RIT (Routing Information Table) location, which includes
 - New VPI/VCI to be added to an outgoing cell
 - Output port address indicating to which port the cell should be routed
 - Priority field allowing the switch to selectively send cells to output ports or discard them (in case of buffer overflow)

-
- Three routing modes:
 - Unicast
 - multicast
 - broadcast
 - In multi-cast/broadcast case, a cell is replicated into multiple copies and each copy is routed to its intended output port/outbound VC
 - ATM connections are either
 - Pre-established - Permanent Virtual Connections (PVCs)
 - Dynamically set up - Switched Virtual Connections (SVCs)
 - Signaling (UNI or NNI) messages carry call set up requests to ATM switches
 - Each ATM switch includes a call processor, which
 - processes call requests and decides whether the requested connection can be established
 - updates Routing Information Table based on established and released call connections
 - Ensuring that VPIs/VCIs of cells, which are coming from several inputs and directed to a common output are different
 - finds an appropriate routing path between source and destination ports

ATM SWITCH CHARACTERISTICS

- ❑ High-Speed Interface (50Mbps to 2.4 Gbps)
- ❑ Transports various types of traffic, each with different requirements
 - Cell loss
 - Errors
 - Delay and Delay jitter
- ❑ Relays (routes and buffers) cells from input to output ports
- ❑ Provide control and management functions
- ❑ Supports a set of traffic control requirements

MAIN FUNCTIONAL BLOCKS OF AN ATM SWITCH



- LIC - Line Interface Card
- IPC - Input Port Controller
- OPC - Output Port Controller

FUNCTIONAL BLOCKS OF AN ATM SWITCH

Main blocks :

- **Line interface cards (LICs)**, which implement input and output port controllers (IPCs and OPCs)
- **Switch fabric** provides interconnections between input and output ports
- **Switch controller**, which includes
 - A call processor for Routing Information Table manipulations
 - Control processor to perform operations, administration and maintenance functions for switch fabric and LICs

The common goals of all ATM switches:

- Switch all cells with as low a *discard rate* as possible.
- Cell arriving on a virtual circuit in a certain order must also depart in that order.

ATM SWITCH

- ❑ A problem occurs when the cells arriving at two or more input lines want to go to the same output port in the same cycle.
- ❑ One solution is to provide a *queue for each input line*. If two or more cells conflict, one of them is chosen for delivery, and the rest are held for the next cycle.
- ❑ The choice can be made at random, or cyclically, but should not exhibit systematic bias.

FUNCTIONS OF INPUT PORT CONTROLLER

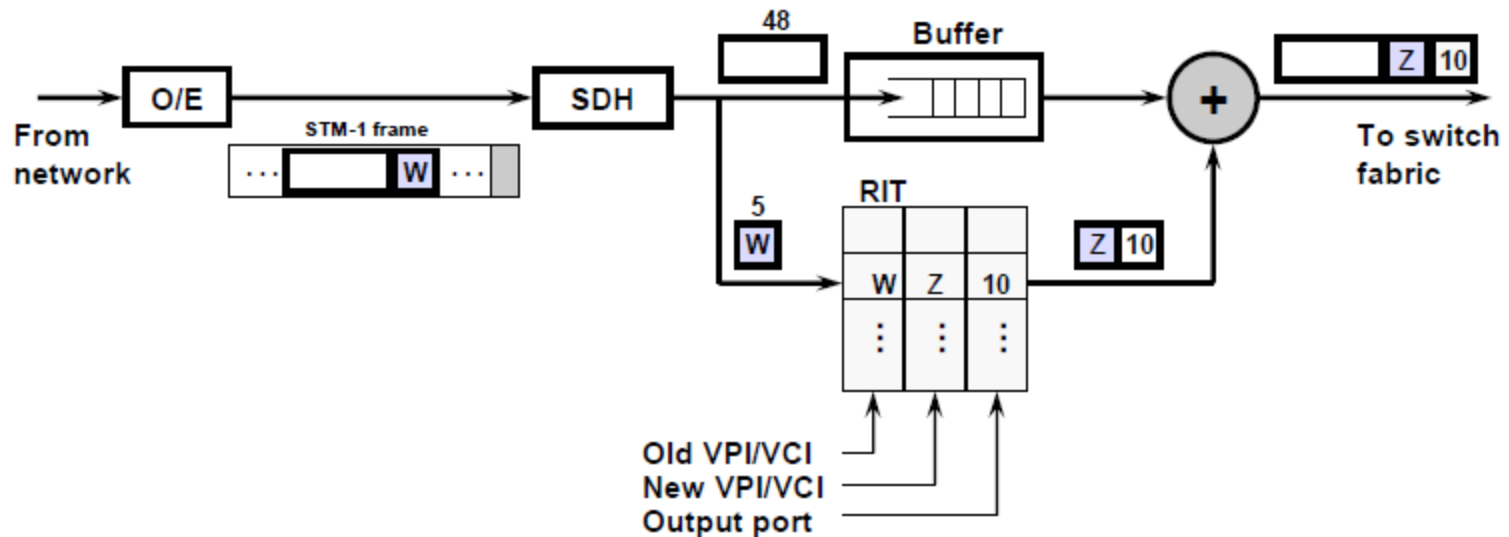
- Line termination and reception of incoming line signal
- Extraction of cell header for processing
- Storing of cell payload (or whole cells) to buffer memory
- Head Error Control (HEC) processing
 - => discard corrupted cells
 - => forward headers of uncorrupted cells to routing process
- Generation of a new cell header and routing tag to be used inside switch fabric
- Cell stream is slotted and a cell is forwarded through switch fabric in a time-slot

FUNCTIONS OF OUTPUT PORT CONTROLLER

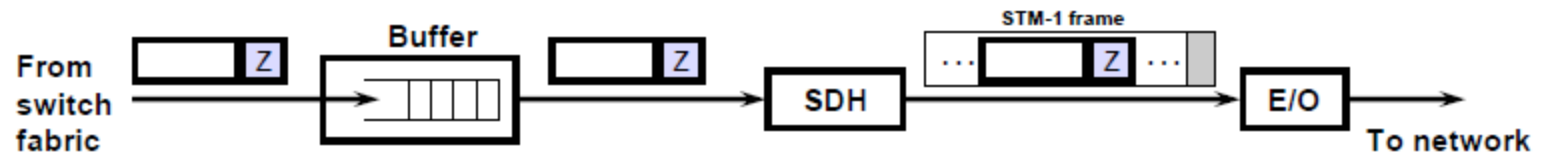
- Cells received from switch fabric are stored into output buffer
- Generation of a new cell header.
- One cell at a time is transferred to the outgoing line interface
- If no buffering available then contention resolution
=> one cell transmitted and others discarded
- If buffering available and priorities supported then higher priority cells forwarded first to transport frame processing
- Cell encapsulation into transport frames.
- Transmission of outgoing line signal

INPUT AND OUTPUT CONTROLLER

Input controller blocks:



Output controller blocks:



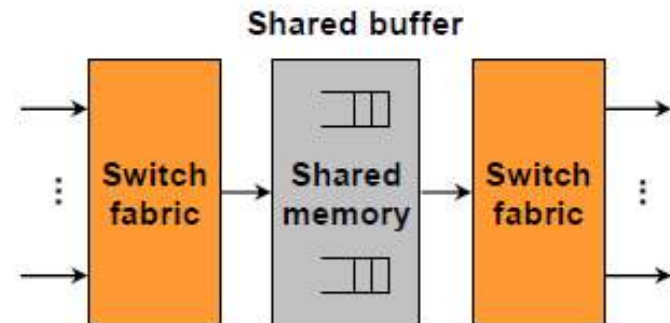
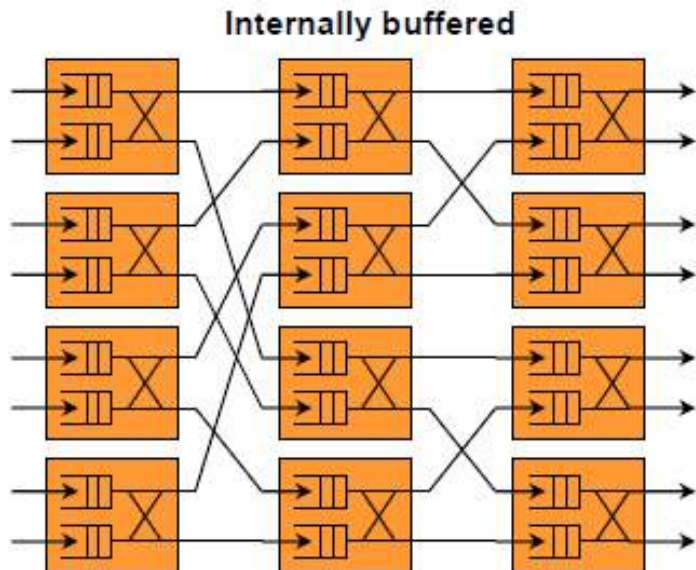
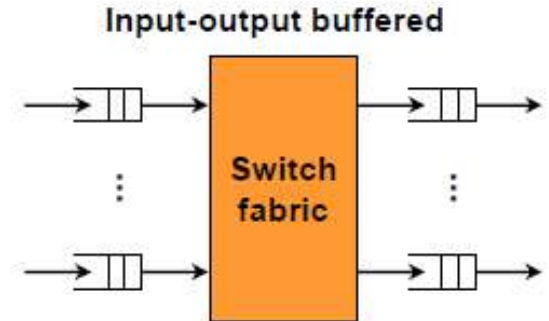
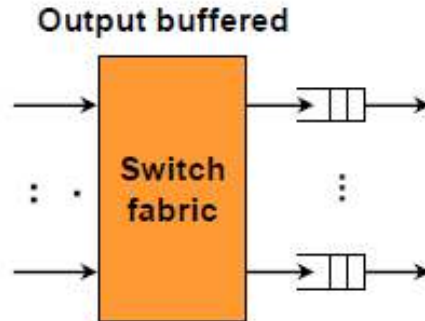
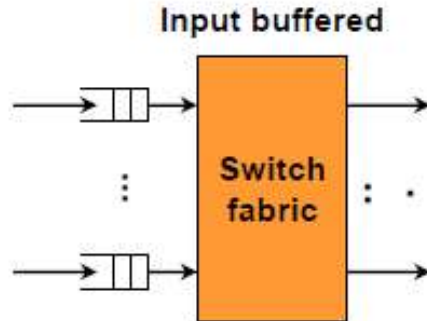
SWITCH CONTROL

- Switch controller implements functions of ATM management and control layer
- **Control plan**
 - Responsible for establishment and release of connections
 - Signaling/management used to update routing tables in different switches
 - Processes Operations Administration Management cells

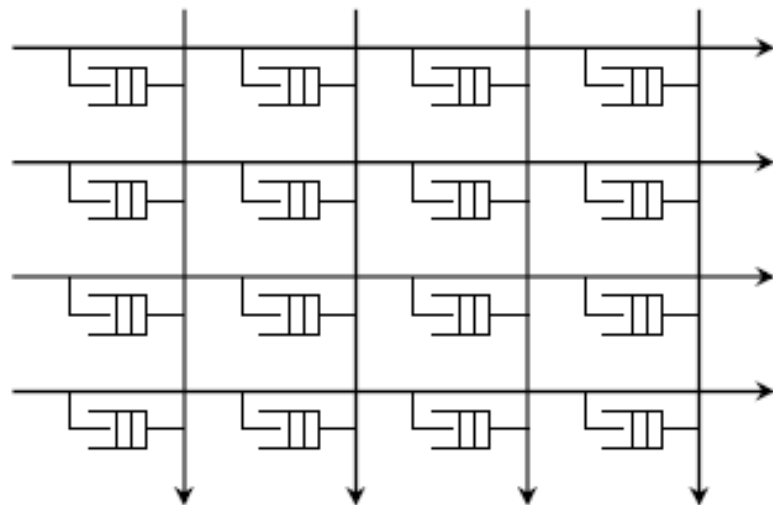
ATM SWITCHING AND BUFFERING

- Due to asynchronous nature of ATM traffic, buffering is an important part of an ATM switch fabric design
- A number of different buffering strategies have been developed
 - input buffering
 - output buffering
 - input-output buffering
 - internal buffering
 - shared buffering
 - cross-point buffering
 - recirculation buffering
 - multi-stage shared buffering
 - virtual output queuing buffering

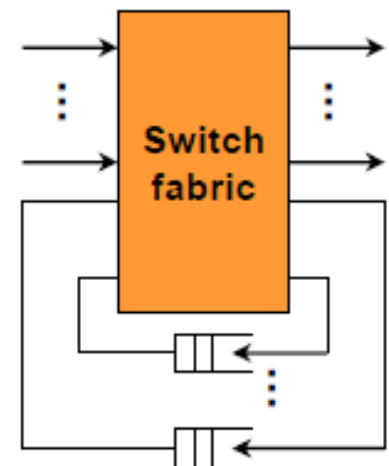
BUFFERING STRATEGIES



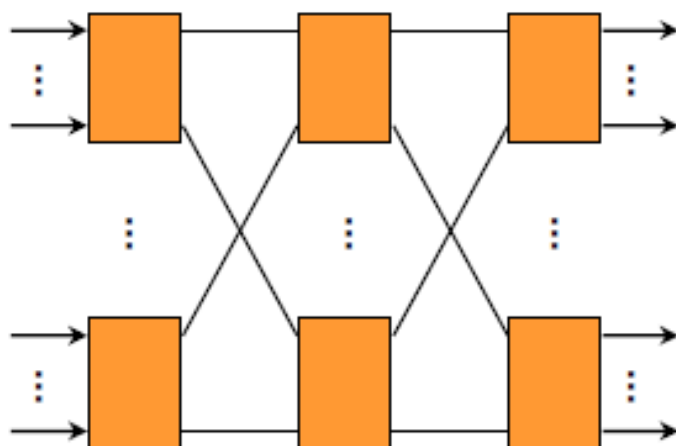
Cross-point buffered



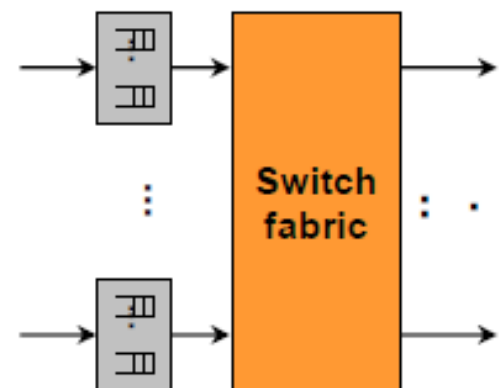
Recirculation buffered



Multi-stage shared buffer



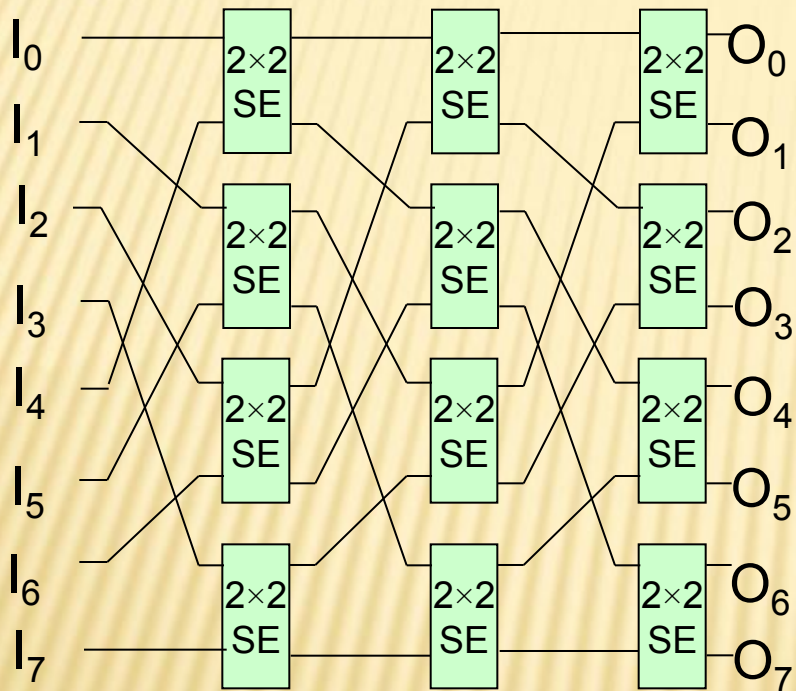
Virtual output queuing



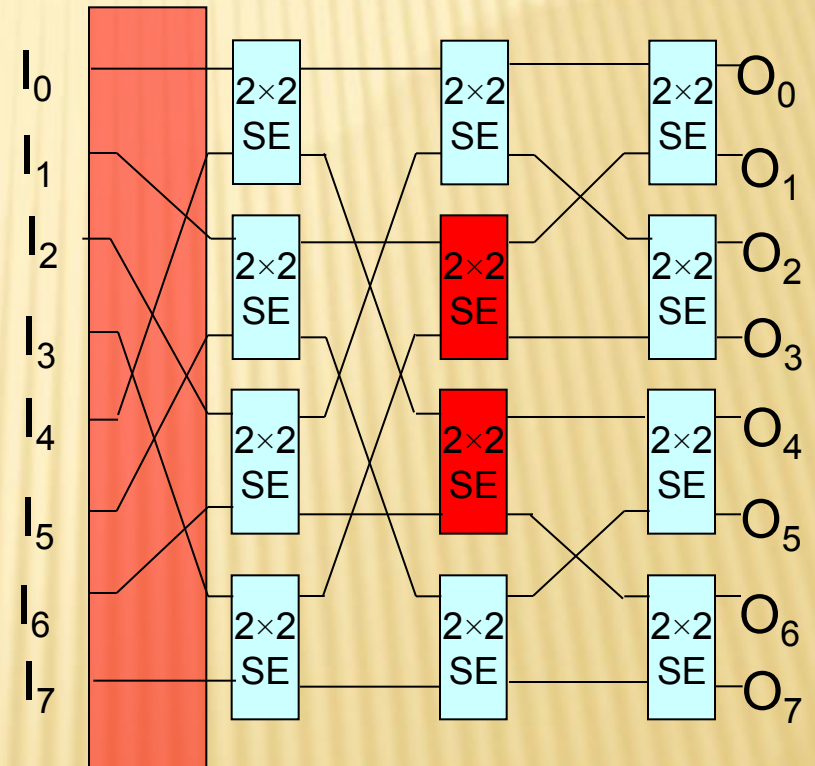
ATM SWITCH

- ❑ The problem with input queuing is that when a cell has to held up in the case of the output blocking, it blocks the progress of any cells behind it. This is called **head-of-line blocking**.
- ❑ The other solution that does not exhibit head-of-Line blocking is to have a *queue for each output line*.
- ❑ When two cells want to go to the same output line in the same cycle, both are passed through the switch. One of them is put on the output line, and the other is queued on the output line.

ATM SWITCH – THE BATCHER-BANYAN SWITCH

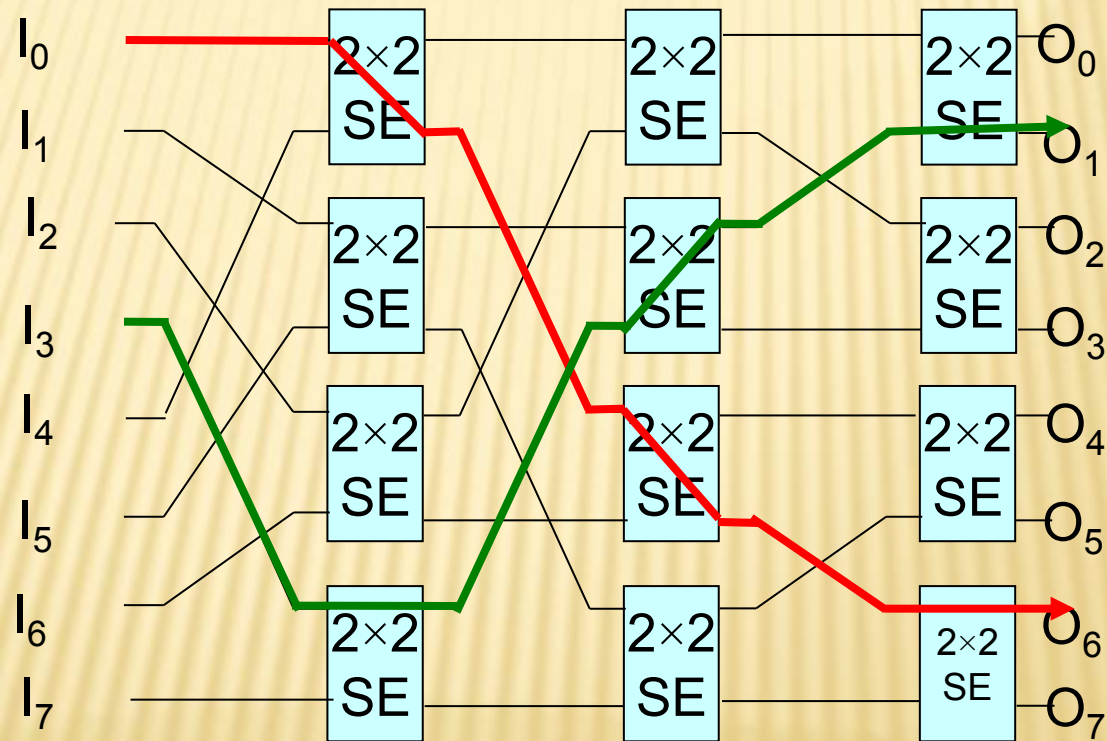


Omega Network



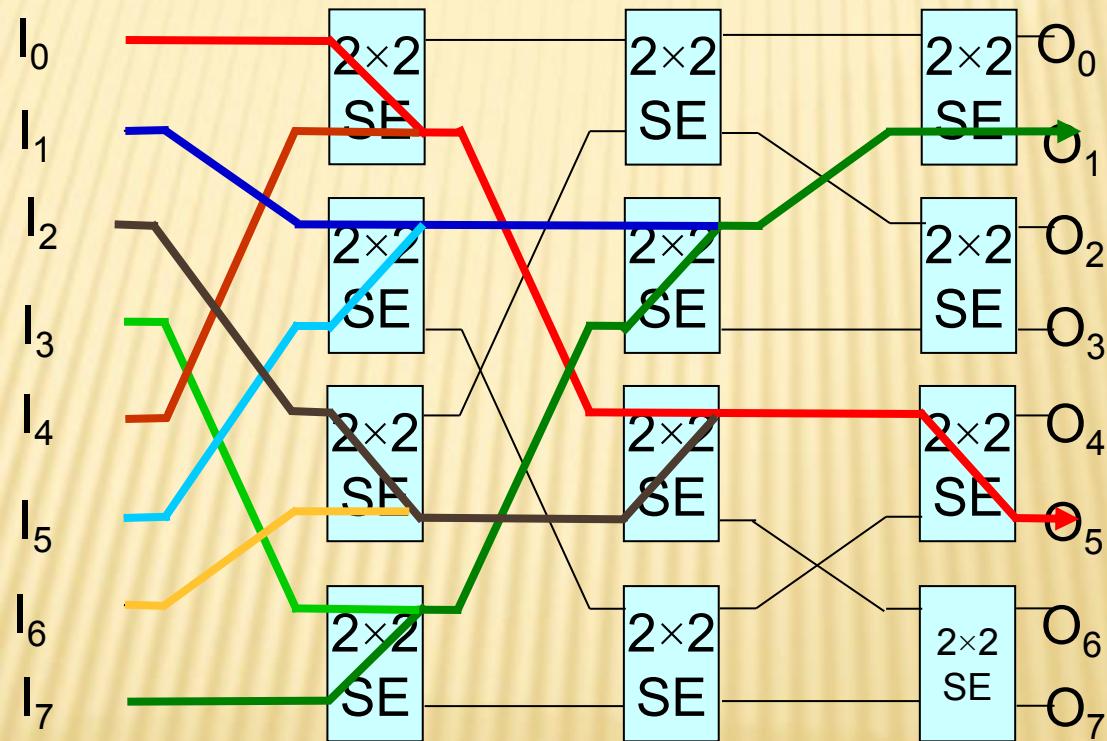
Banyan Network

ATM SWITCH – THE BATCHER-BANYAN SWITCH



Self-Routing in a Banyan Switch

ATM SWITCH – THE BATCHER-BANYAN SWITCH



Cells Colliding in a Banyan Switch

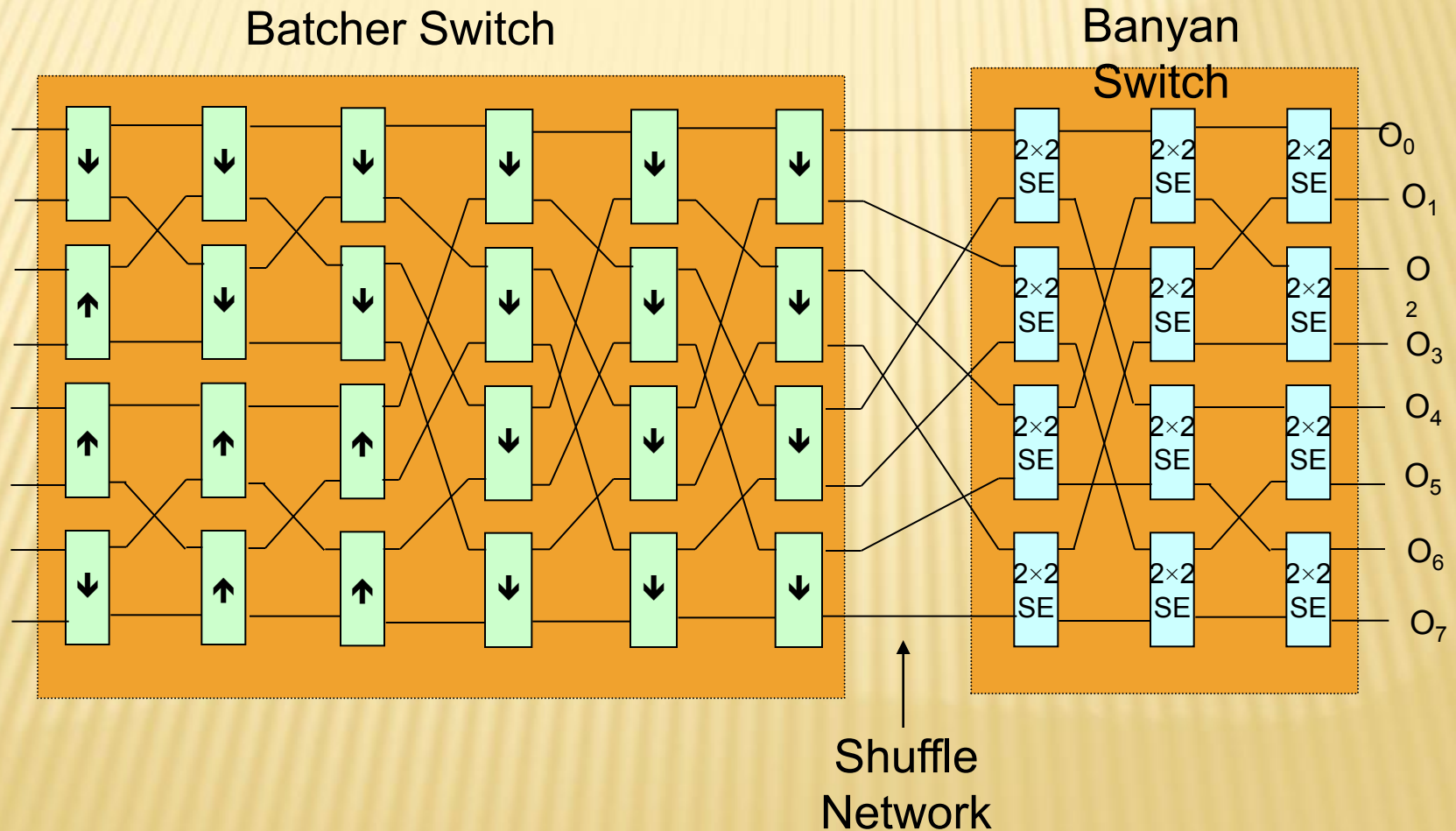
ATM SWITCH – THE BATCHER-BANYAN SWITCH

- ❖ The idea behind the *Batcher-Banyan switch* is to put a *Batcher switch* in front of the Banyan switch to permute the cell into configuration that the banyan switch can handle without loss.
- ❖ A Batcher switch is synchronous and works with discrete cycles.
- ❖ A Batcher switch is built up of 2×2 switching elements.
- ❖ When a switching element receives two cells, it compare their output addresses numerically and *routes the higher one on the port in the direction of the arrow*, and the lower one the other way.

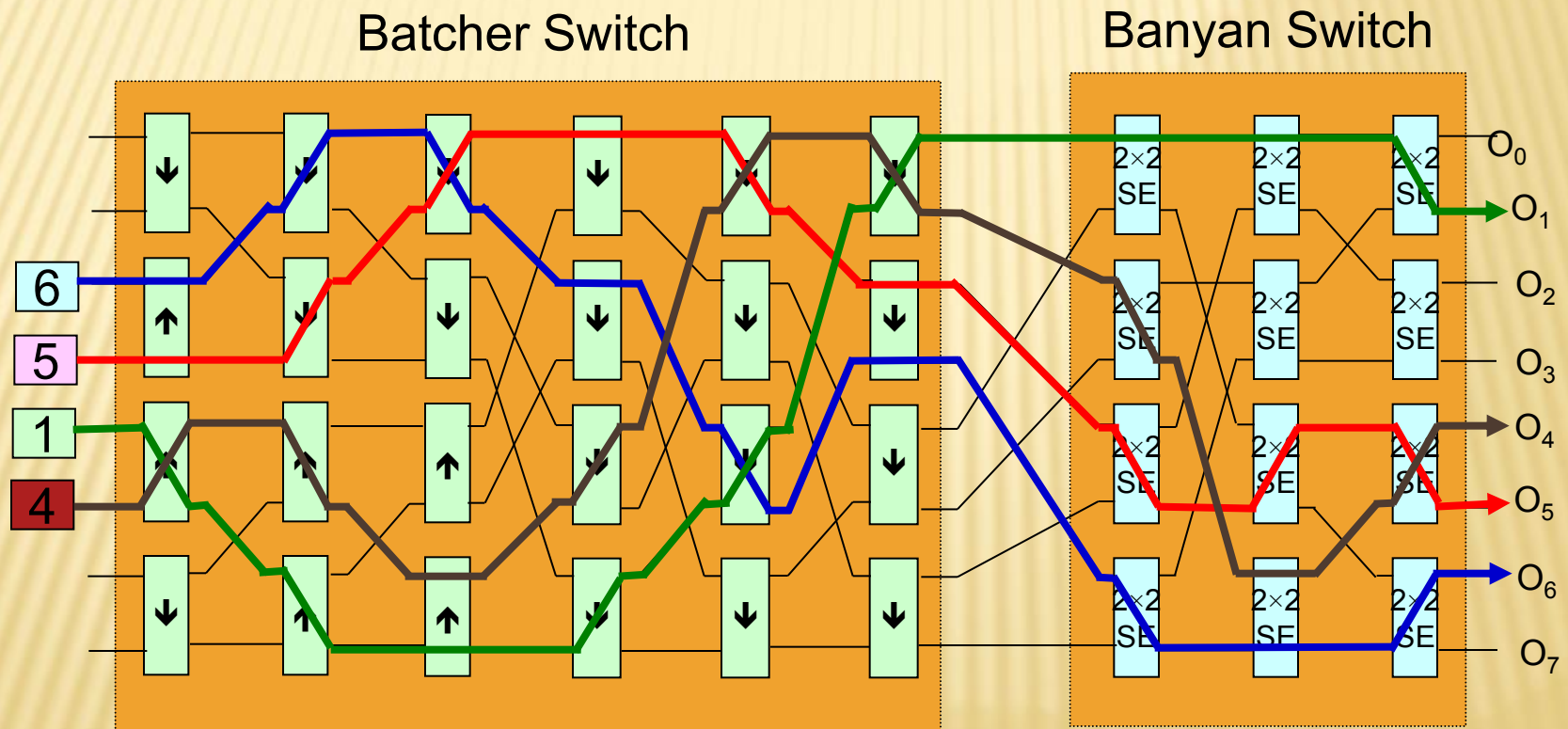
ATM SWITCH – THE BATCHER-BANYAN SWITCH

- ❑ When k cells are present on the input lines, the Batcher switch puts the cells in sort order on the first k output lines.
- ❑ After exiting the Batcher switch, the cells pass through a shuffle connection and are then injected into a Banyan switch.
- ❑ The final result is that every cell appears on the correct output line at the end of the Banyan switch.

ATM SWITCH – THE BATCHER-BANYAN SWITCH



ATM SWITCH – THE BATCHER-BANYAN SWITCH



HIGH PERFORMANCE SWITCHES

- ❑ High performance switching is necessary to match the high speed networks.
- ❑ We can classify the switches by:
 - ❖ Multiplexing techniques
 - ❖ Packet versus circuit switching
 - ❖ Synchronization techniques
 - ❖ Internal blocking/output blocking versus non-blocking
 - ❖ Unicast versus multicast
 - ❖ Single-stage versus multistage switching

Multiplexing Techniques:

- ✗ Time Division Multiplexing (**TDM**)
- ✗ Wavelength Division Multiplexing (**WDM**)
- ✗ Code Division Multiplexing (**CDM**)
- ✗ Space Division Multiplexing (**SDM**)

Packet versus Circuit Switching:

- ❖ In *circuit switching*, a dedicated line is set up before transmission and is occupied by the user who made that call until the service is terminated. The delay and throughput are constant.
- ❖ In *packet switching*, there is no dedicated line, and messages are divided into packets which may be sent on different paths; reassembling is needed in the destination. The delay and throughput varies.

Packet versus Circuit Switching:

- ❑ In high-speed networks, only packet switching is considered because of the following reasons:
 - Packet switching can dynamically use the resources but circuit switching has constant delay and throughput.
 - Packet switching is more suitable for integrated voice, video, and data services. Each packet is treated the same way whether it is voice, video, or data packets.

Synchronization Techniques:

- ❑ There are two types of synchronization:
 - ❖ **Synchronous Switching:** To send a message according to a certain time schedule.
 - ❖ **Asynchronous Switching:** To send a message at any desired time.
- ❑ Since the asynchronous switching is more flexible and can use the network resources dynamically. Therefore, high-speed networks usually use asynchronous switching.

Blocking versus Non-Blocking:

- ✖ Switches may be categorized according to whether the packet are blocked while switched:
 - + **Blocking:** Blocking may be due to either *internal blocking* or *output blocking*.
 - ✖ **Internal Blocking:** Packets (cells) collide within a switch when more than one cell tries to use the same internal link, even though they are destined for different output **at the same cycle**.
 - ✖ **Output Blocking:** More than one cell is destined for the same output **at the same cycle**.
 - + **Non_Blocking:** Neither internal/output blocking has occurred.

Unicast versus Multicast:

- ✘ A *unicast switch* is a point-to-point switch, with only one destination per transmission.
- ✘ If there are more than one destination, it is *multicast switch*.
- ✘ Multicast switch is more complicated than the unicast switch.
- ✘ It is necessary to have one-to-many or many-to-many connection for future high performance switches.

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Single-Stage versus Multistage Switching:

- ✖ *Single-stage switching* offers a structure to prevent internal blocking, but requires numerous *cross-points*.
- ✖ *Multistage switching* offers a simpler structure and can be implemented economically because only a small number of cross-points are needed; however, a remedy for internal blocking is required.

COMPARISON OF SWITCHES

Network		Internal Blocking	Output Blocking	HOL Blocking	Multiplexing
Multi-Stage	Banyan	Y	Y	N	SDM
	FIFO input queue Banyan	N (By buffering arriving packets)	N	Y	SDM
	FIFO output queue Banyan	Y	N	N	SDM
	Batcher-Banyan	N (By sorting arriving packets)	Y	N	SDM
Single-Stage	Point-to-point (crossbar)	N	Y	N	SDM
	Broadcast (knockout)	N	Y	N	SDM